HITACHI ANALOG COMPUTER 505 OPERATION MANUAL

Hitachi, Ltd.

HITACHI ANALOG COMPUTER 505

CONTENTS

"HITACHI ANALOG COMPUTER PROGRAM MANUAL" will explain the programming technique for HITACHI 505 Computer.

The Manual is common in programming for all kinds of HITACHI Analog Computer.

ILLUSTRATIONS

SECTION I

INTRODUCTION

Many scientific problems studied today in various fields involve the solution of partial or ordinary differential equations. It is the exception, rather than the rule, that the problems admit exact analytic solutions. The modern analog computer, such as the Hitachi 505, provides a convenient method for obtaining numerical solutions to such problems as well as enabling the scientist to study the effect of changes in the physical system.

The method of problem solution in an analog computer is quite simple. The computer is used to "build" an electronic analogy which obeys the same set of differential equations as the physical problem to be studied. Once this model has been constructed, experiments may be performed on this model in lieu (INSTEAD OF) of experiments on the physical system. Investigations which might be difficult to carry out on the actual system become quite feasible with this technique. For example, a physician may wish to study the effect on blood pressure in a certain portion of the brain in the event that a patient loses an arm. It is unlikely that this experiment would be performed by any means other than simulation!

Since the analog computer "models" the problem, each problem variable corresponds to, or is analogous to, a computer voltage. As these voltages are readily available for measurement, instrumention (INSTRUMENTATION) is employed to measure the problem variables as in an actual system. Solutions may be continuously displayed on a readout oscilloscope, permanently plotted on a strip chart or x-y plotter, or numerically

evaluated by means of a voltmeter or digital voltmeter.

The detailed steps necessary for problem solution will be discussed in detail in a later section. Briefly, one must first construct a mathematical model for the system to be studied. Often such a model is not available. In this case, there are analog computer techniques available for generating a model from data taken from the physical system. The next step involves the construction of a computer "block diagram" (an array of summing amps, integrators, etc.) which obeys the same differential equations as the system model. This diagram is then used to connect computing elements utilizing the patchboard. Since the patchboard may be removed from the computer and another patchboard inserted, it is not necessary to use computer time othersthan for actual computation.

The problem is now ready for computer solution. After mounting the proper patchboard, the potentiometers ("Pots") are set to correspond to the physical problem constants. The computer solution is now obtained by pressing the "COMPUTE" button. Problem variables may then be observed and recorded as desired. Additional runs may be made with different physical constants, problem variables, initial conditions, etc.

This manual describes the computer operation and programming in detail. It should be emphasised that a knowledge of electrical engineering is not necessary to success fully operate an analog computer. The block diagram approach used in this manual is common in many fields. The manual describes the general computer operating controls first. This is followed by a module by module description of each "black box",

including its input-output characteristics and photographs of actual patchboard connections. Basic programming is explained in the program manual at an introductory level. The detailed example given in this section may be used as a model for the user's particular problem set up in the manual, titled "Applications", explains the special features of the Hitachi 505 for more advanced techniques. It includes function generation, transfer function simulation, and partial differential equation solution. Helpful suggestions for the use of the automatic operation unit in optimization problems and the Timer and Logic Operations board in iterative methods is also included.

SECTION II

THE HITACHI 505 COMPUTER

1. GENERAL DESCRIPTION OF HITACHI 505

The Hitachi 505 is a medium size desk-top general purpose analog computer having a wide variety of applications. This computer may be installed in any office or laboratory without special considerations as to power or temperature control. The power consumption is quite low, easily handled by normal office wiring. Since this computer supplies its own internal operating environment by means of an oven, it does not depend on an accurate external temperature control. The heat delivered to the room by the unit itself is about the same as that delivered by a medium size laboratory oscilloscope.

The Hitachi 505 is modular in concept with solid state components used throughout*. The modular arrangement of the computer permits special machine configurations depending on the user's requirements. The component arrangement allows simplified wiring. Color coding of the modules aids in rapid identification of elements and simplifies wiring checks.

The computer is housed in two cabinets, the computer main frame and the control console. These units may be easily separated for transportation. The main computer console contains the patchboard with the associated computing components mounted in an oven directly behind the patchboard. Beneath the patch panel is a panel containing the amplifier overload indicators, the readout addressing system, and the coefficient potentiometers with their associated indicator lamps,

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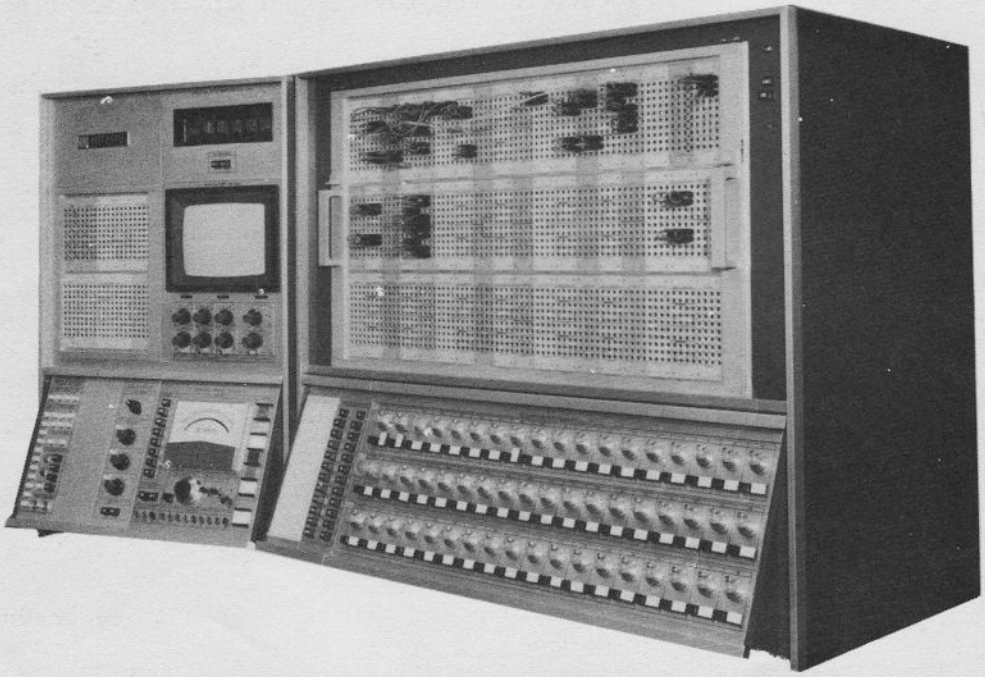
* With the exception of the oscilloscope tube and a high voltage rectifier in it.

addressing buttons, and label plates. A control located immediately to the left of the patchboard operates the motor drive for removing or replacing the patchboard. The lower panel of the main computing console is tilted toward the operator for ease of operation.

The power supply for the computing elements is located in the bottom rear of the cabinet. It is easily removed for service or transportation.

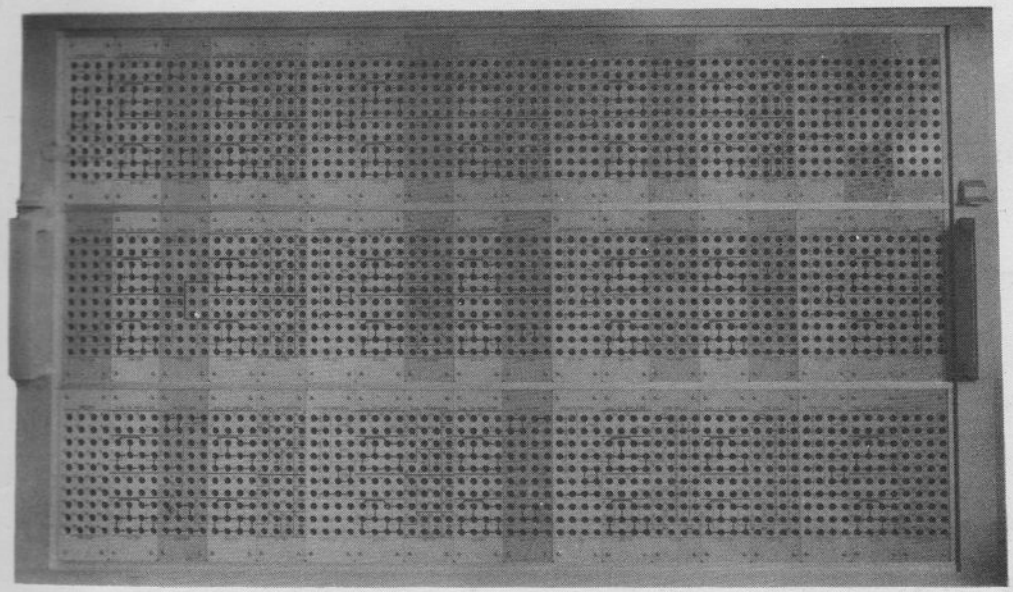
The control console contains the control panel, the oscilloscope, the iterative operation timer, the digital logic unit, and the digital voltmeter. The control panel, located in the lower right hand side of the control console, contains the manual mode control switches, a voltmeter, the reference potentiometer, and some external trunk terminals. Immediately above this unit is a three channel oscilloscope with electronically generated scales. The digital voltmeter mounted above this oscilloscope may be used for accurate potentiometer setting and solution readings. The iterative operation timer, which may be used for sequential mode control, is located in the lower left corner of the control console. The digital logic unit, mounted directly above the timer module, contains various types of patchable logic.



NOTES: 1. THE DISPOSITION CHANGED SLIGHTLY IN THE LATER PRODUCTS.

2. ONE MORE COMPUTING CONSOLE MAY BE ADDED TO THE RIGHT OF THE ABOVE COMPUTER.

FIGURE 2.1-1 TYPICAL 505, FRONT VIEW



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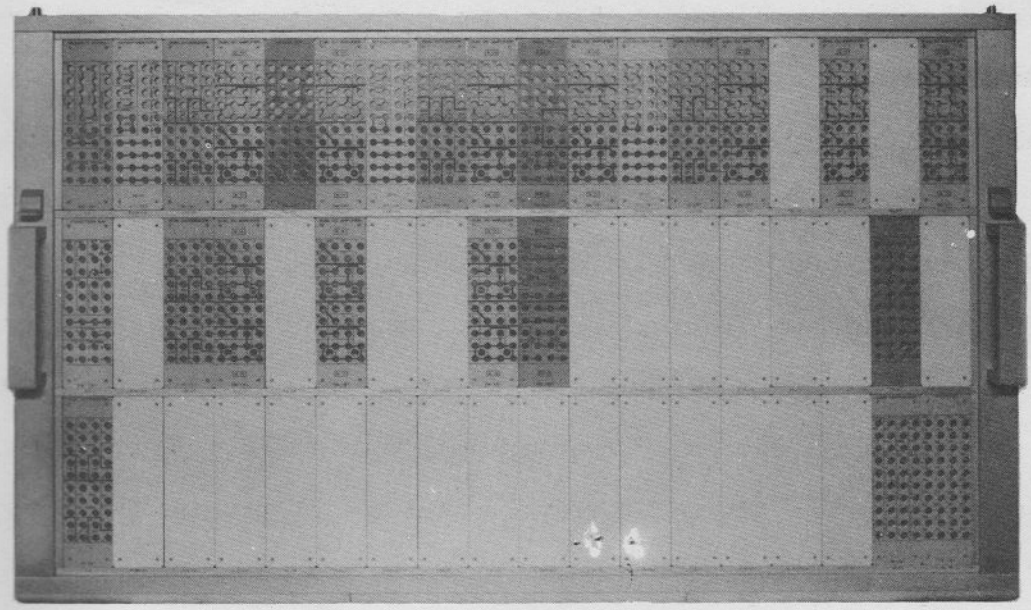

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FIGURE 2.1-2 PRE-PATCH PANEL MODULAR LAYOUT

2. OPERATING CONSIDERATIONS

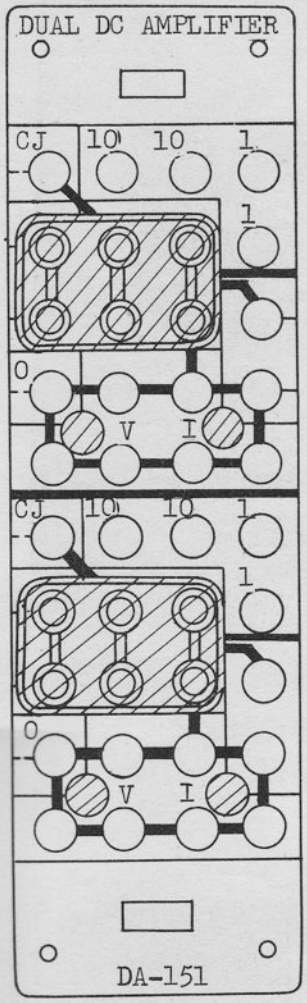
The Hitachi 505 (Figure 2.1-1) is shipped complete with all components in place except power supply and DVM. Each unit is completely calibrated and adjusted at the time of manufacture. After performing the simple installation and check procedure outlined in the maintenance manual, and connecting the unit to a suitable power source, the computer is ready for operation.

The current limiting circuits protect the reference supplies and all active operational elements from damage due to shorting to ground, or to each other. Thus an errant patching connection (shorting the plus reference to ground for example) will not adversely effect the supplies (output current drops to zero) nor will the reference supply fuse blow. In addition, the surface of Pre-Patch Panel is covered with coloured plastic plates (except frame and handles) reducing shorting-out of hanging patch cords.

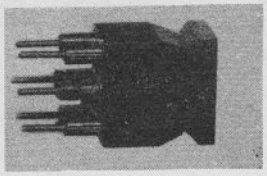
a. Preliminary Operating Considerations

The following steps are recommended prior to operating the Hitachi 505 to prevent possible false trouble indications.

(1) Ascertain that each operational amplifier has a six connector bottle plug or a combination of bottle plugs equal to a six connector bottle plug, properly placed and seated as shown in Figure 2.2-1. This provides the amplifiers with feedback and prevent them from overloading during the problem solution.

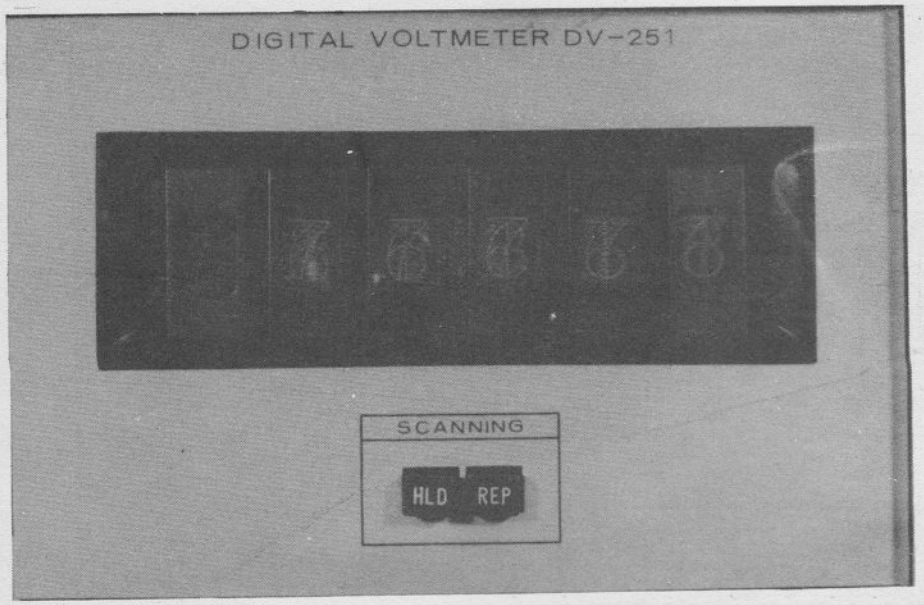


(a)



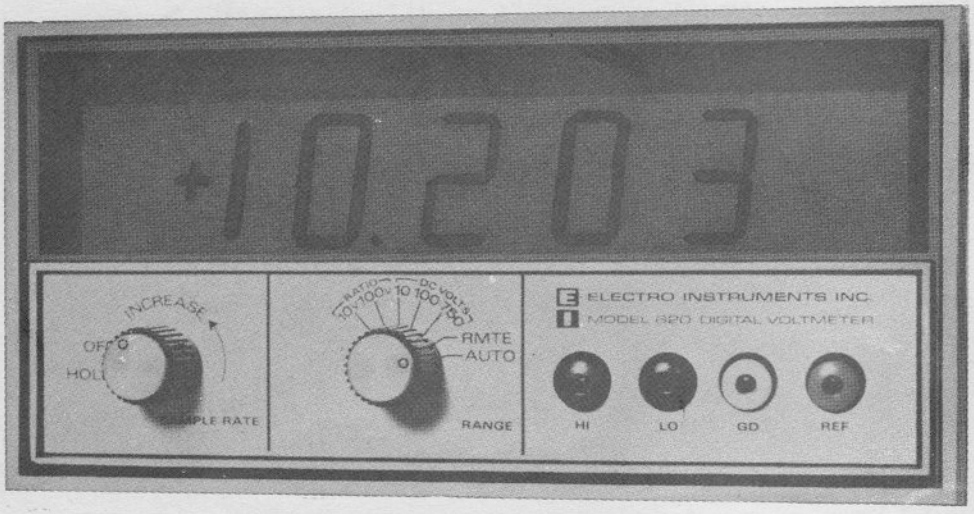
(b) SIX-CONNECTOR BOTTLE-PLUG

FIGURE 2.2-1 AMPLIFIER WITH SIX CONNECTOR BOTTLE-PLUG PROVIDING FEEDBACK



DVM DV-251

("RATIO-VOLT" SWITCH ADDED IN LATER MODEL)



DVM E1 620

FIGURE 2.2-? DVM FRONT VIEW

The procedure for inserting and removing the Pre-Patch Panel is described in Paragraph 2.b.

(2) Patch the Digital Voltmeter (DVM) and multi-range voltmeter (VM) to the selector readout system. (See Figure 2.3-2 and Paragraph 2.c. of this section for a description of the selector system operation)

(3) Apply power to the computer, then Pot Set mode will appear. Initially the overload lamps of the operational amplifiers will light; after a few seconds all of the lamps should extinguish.

(4) Check the various supply voltages of the computer. All power supply outputs are connected to the voltmeter switch in front of the power supply through appropriate scaling resistors; the check may be accomplished simply and rapidly.

(5) Check the plus and minus reference supplied for readout on the DVM by selecting 100 (red for plus) and 100 (blue for minus). See Paragraph 3.a.

(6) Allow about thirty minutes warm-up time; this assures that the computing components, (including the DVM and oscilloscope) are up to normal operating temperature. Ground the DVM input termination (designated on the OC-151 READOUT PANEL), and confirm the reading is within 000.00 plus or minus one bit. Other adjustment for DVM will be necessary according to Model of DVM, for DV-251, the zero check is the only step necessary to assure the correct operation.

(7) In the POT SET mode of the computer (POT SET button on the control panel, model CT-251 depressed), closed relay contacts provide a feedback circuit for the operational amplifier. (See Paragraph 4 of this section for a more detailed description)

This feature permits the removal of the Pre-Patch Panel to balance the operational amplifier. However, when the computer is switched from POT SET to any other mode, the relay contacts open and the circuits as patched on the Pre-Patch Panel provides the feedback loop. Momentary amplifier overload may result during the relay operating time; thus to eliminate possible error in the computer solution, the operator should always switch the computer RESET (depress the RESET button) or ALL RESET (depress ALL RESET button for multi-mode operation only), before switching to the COMPUTE or REP OP mode. This permit the pot set relays to open and the amplifier summing junctions to settle before starting the problem solution. There is no actural waiting period required; that is, the operator may depress the RESET or ALL RESET button and then immediately depress the button for the desired mode. This sequence of operation will prevent the possible momentary overload from effecting the problem solution.

b. Pre-Patch Panel Insertion and Removal

To insert the Pre-Patch Panel, set the lip on the lower edge of the panel in the quide groove (Figure 2.2-3). Push the top of the panel in so the panel is vertical until the panel is clamped automatically.

Depress the ENG (for ENGAGE) button on the lower left edge of the computing console. This button properly seats and firmly holds the Pre-Patch Panel in position. As the ENG and DIS (for DISENGAGE) buttons can memorize the operator action, it is not necessary to keep the button depressed until the panel is loaded. In the ENG state, after the panel is loaded, the panel can not be removed unless the DIS button is pushed.

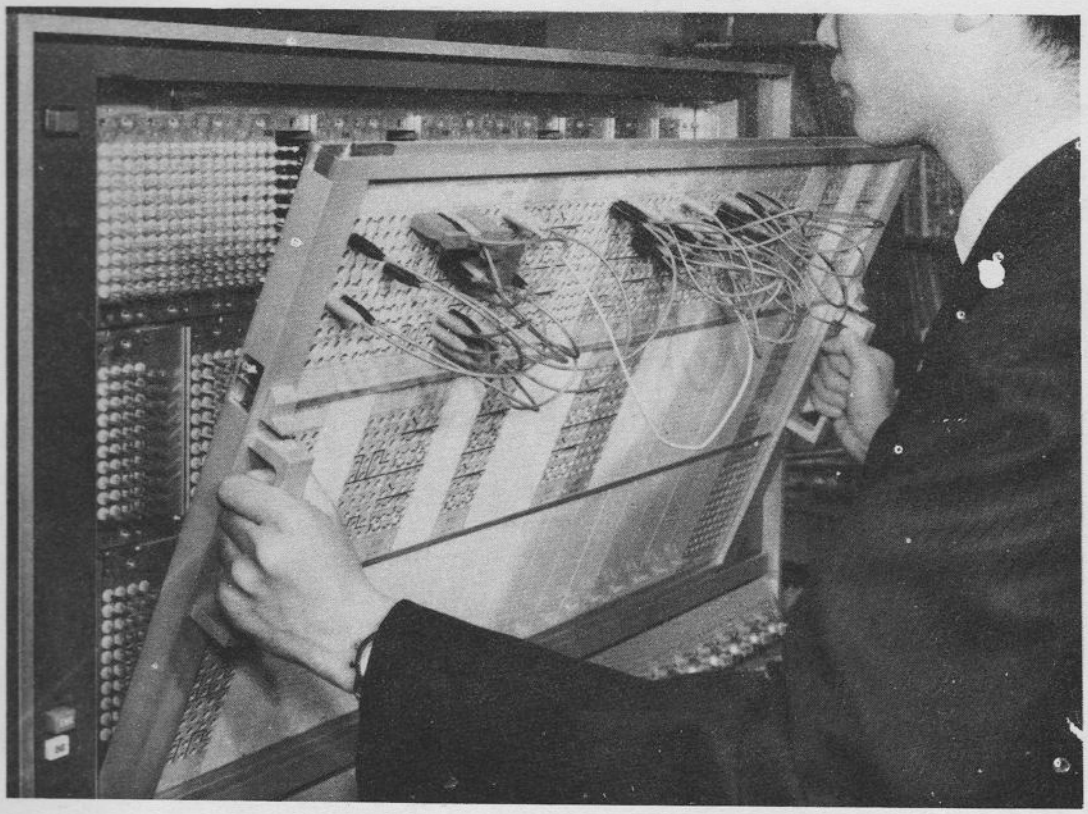


FIGURE 2.2-3 PRE-PATCH PANEL INSERTION

in the ENG state without the panel, the panel can not be loaded. This feature eliminates the possibility of accidentally engaging or disengaging the Pre-Patch Panel.

The removal of the Pre-Patch Panel is essentially the opposite of inserting the panel. Depress the DIS button, and depress the levers on both handle of the panel. Then pull the panel towards the operator upper edge of the panel first.

It is not necessary to keep the panel straight by hand after inserting the panel or after pushing the DIS button.

c. Amplifier Balance

The d-c operational amplifiers are chopper stabilized to prevent drift and resultant errors in the computer results. Drift in an amplifier results in an output voltage (or offset) with a zero input. To eliminate offset, the amplifiers of the 505 are balanced, i.e., with a bias current is applied to the amplifier summing junction equal and opposite to any current due to drift thus placing the summing junction at virtual ground. Once balanced, drift in the amplifiers is eliminated automatically by the stabilizer circuit.

The d-c amplifiers of the 505 are extremely stable and normally do not require balancing for periods up to several months. To assure accuracy and confidence in the computer results, it may be desirable to check the amplifier balance daily; this check can be made rapidly and simply since the selector system and voltmeter are used.

There are two types of amplifier balance in the 505; the voltage balance check and current balance check. Usually, only voltage balance check will be sufficient for each amplifier. The current balance check is necessary to reduce integrator drift, but the operator need not check

it as a daily routine, because current drift is very low and stable.

The following is a step by step procedure for checking amplifier balance.

(1) Place the voltmeter RANGE switch in the (plus or minus) 0.1 position and depress the DIS button of the Pre-Patch Panel control switch. In this state the computer is ready for voltage balance check (BC mode).

(2) Using the selector system, select each amplifier A00 through A39. The voltmeter should register a zero deflection for any other. Two positions of +0.1 and -0.1 of the voltmeter range switch will detect null error in the voltmeter.

(3) Should an amplifier cause a deflection to either side of the center zero on the voltmeter, adjust the corresponding balance control. The balance control for amplifiers A00 through A39 (the operational amplifiers) are located directly behind the Pre-Patch Panel (Figure 2.2-4). There are two balance controls in an amplifier. They are voltage balance control and current balance control. In the BC mode (when DIS button pushed), only the voltage balance is necessary. Adjust these controls for a zero reading on the meter. The current balance should be done for integrator connection amplifiers in HOLD mode.

d. Changing Computational Components

In the solution of some problems it may be necessary to add a specific type of computational component to the existing complement. Since many of the module positions are designed to handle more than one type of computing component, a component not required in the problem investigation may be removed and another unit placed in that cradle.

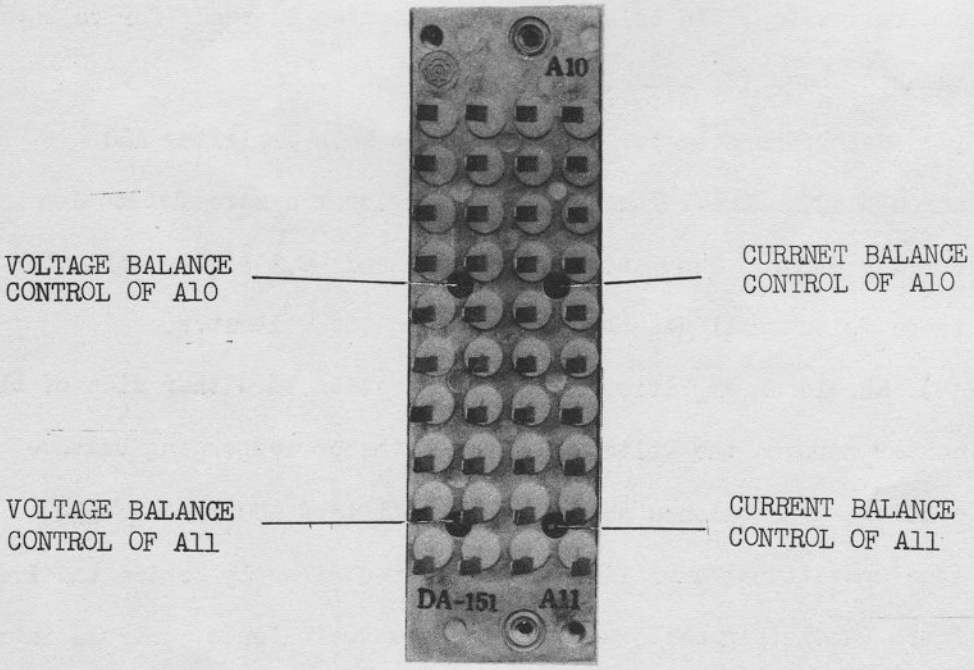
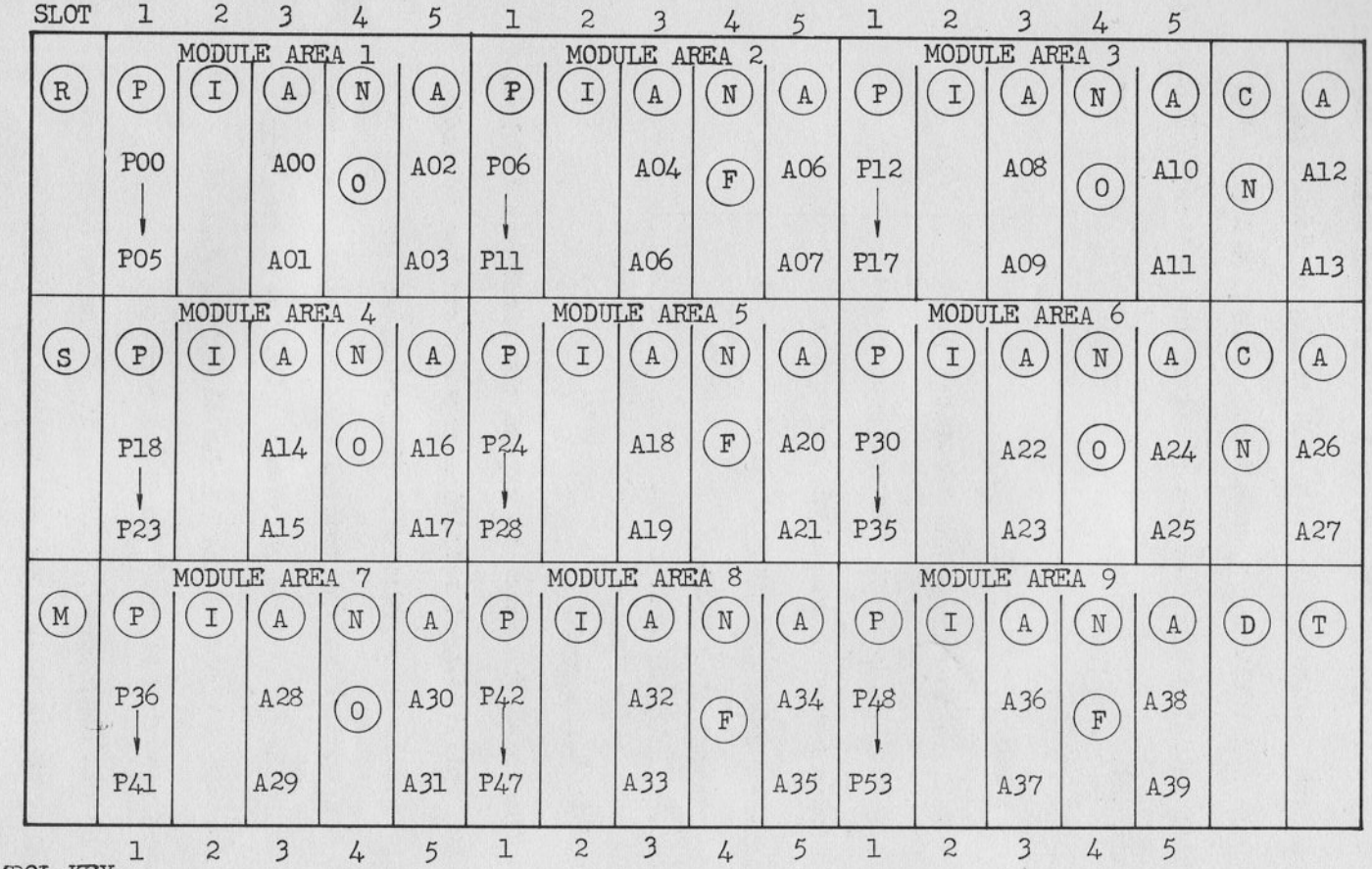


FIGURE 2.2-4 AMPLIFIER BALANCE CONTROL LOCATION



SYMBOL KEY

A	DUAL DC AMPLIFIER	DA-151	N	NON-LINEAR ELEMENT	EM-151, etc.
C	QUAD COMPARATOR	CP-151 OR CP-152	O	AUTOMATIC OPERATOR	AO-151
D	FREE DIODES	FD-151	P	POTENTIOMETERS	PT-151
F	VARIABLE FG	FG-151	R	READOUT PANEL	OC-151
I	DUAL INTEGRATOR TRANSFER DELAY	IN-151 TD-151	S	FUNCTION SWITCH	FS-151
M	MODE CONTROLLER	MC-151	T	TRUNKS	TR-151

FIGURE 2.2-5 COMPUTER COMPONENT MODULE ASSIGNMENT AREAS

Figure 2.2-5 illustrates the various positions of the computing components in the 505 module area. This diagram illustrates which type of computing component is compatible with each cradle or module position. The procedure for replacing a computer component and changing the Pre-Patch Panel patching block is described in the following Sub-Paragraphs (1) and (2).

> NOTE
>
> Failure to change the Pre-Patch Panel patching block may prevent proper use of a computer component due to the arrangement of jumpers on the rear of the patching block.

(1) Computing Module Replacement

(a) Remove the Pre-Patch Panel to expose the component modules, Remove the two phillips-head retaining screws from the top and bottom of the module to be removed. (Figure 2.2-6)

(b) Insert the special module removal handle in the holes provided next to screw holes from which the screws were removed. Attach the two screw knobs on the handle tightly. Pull the module forward removing it from the 505 console.

(c) Place the new component in place. It is easier to insert the new module, if the handle is attached on the front of it. Be sure the guide pin is properly seated in the guide rail before mating the connectors at the rear of the module.

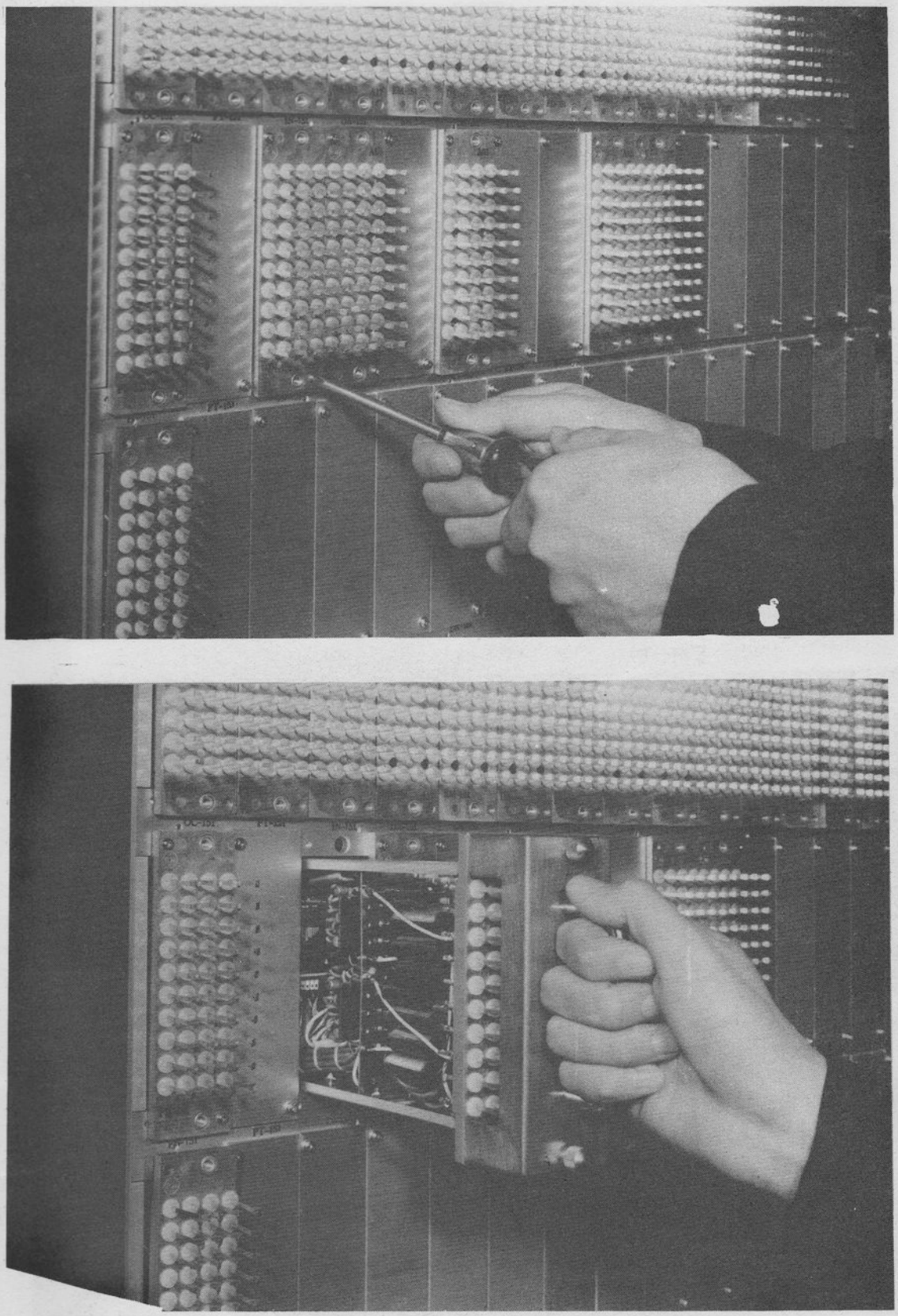


FIGURE 2.2-6 REMOVAL OF COMPUTING MODULE

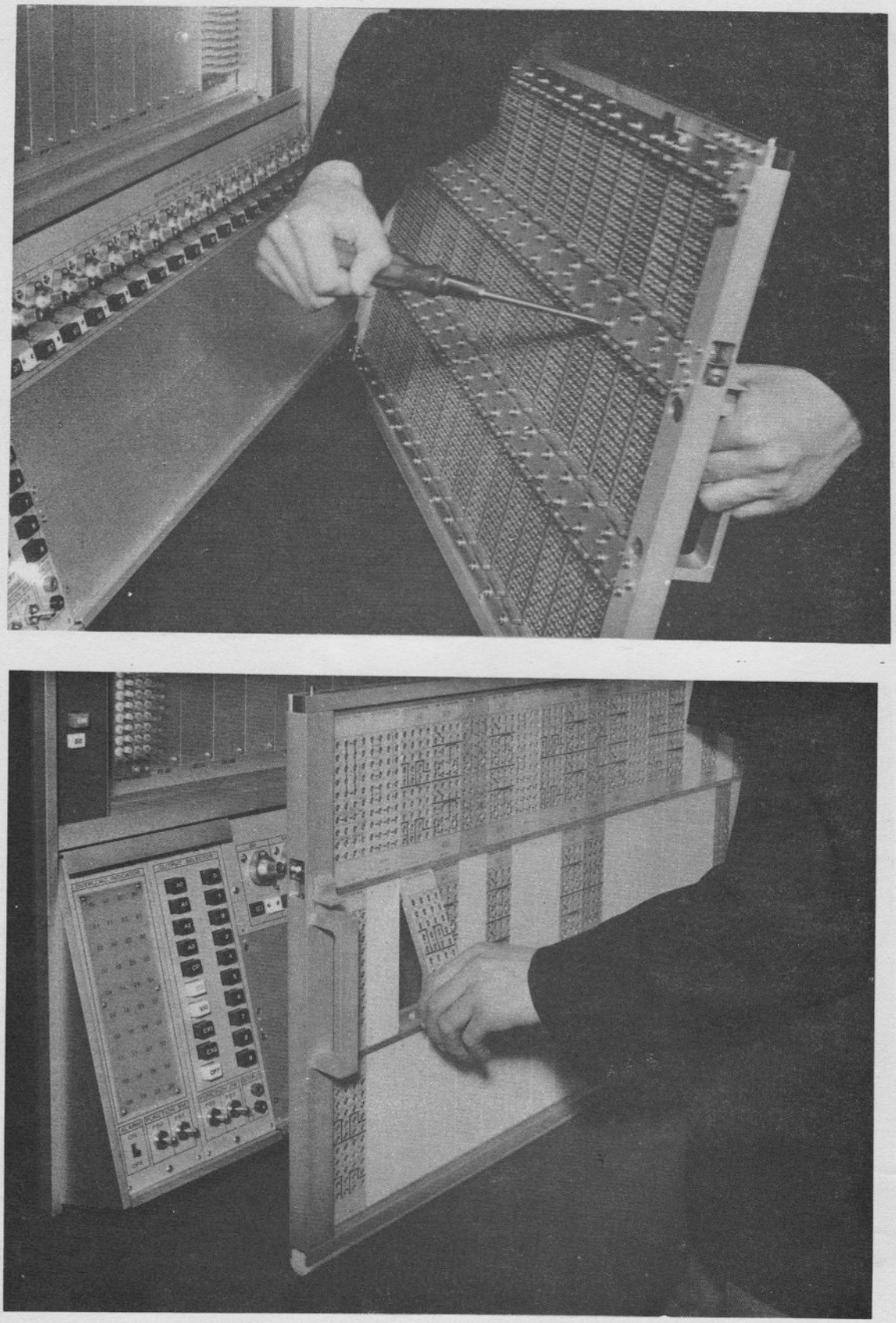


FIGURE 2.2-7 PATCHING BLOCK REPLACEMENT

(d) Check that the module is properly installed (connector firmly mated, etc.) and replace the two retaining screws.

(2) Patching Block Replacement

(a) The Patching blocks of the computing components are held securely in place by the retaining screws on the rear of the Pre-Patch Panel (Figure 2.2-7)

(b) The retaining screws are located on both ends of the patching block. Release them with a screw driver.

(c) Once the retaining strip is free, remove the original block and replace it with the new block. Replace the two retaining screws. The Pre-Panel is now ready for problem patching.

3. MONITORING AND CONTROL

The control system of the HITACHI 505 is designed to allow simple control and monitoring of the computer components (Figure 2.3-1). The following sub-paragraph describes the function and operation of the various monitoring and control facilities of the 505.

a. Output Selector SL-251

The output selector mainly consists of two rows of push-buttons; The first row contains 4 buttons designated A0 through A3, and the second row contains 10 buttons designated 0 through 9. Depressing the A0 button permits the operator to select the outputs of the 10 operational amplifiers (A00 through A09). In the same way, depressing the CP button in the first row permits

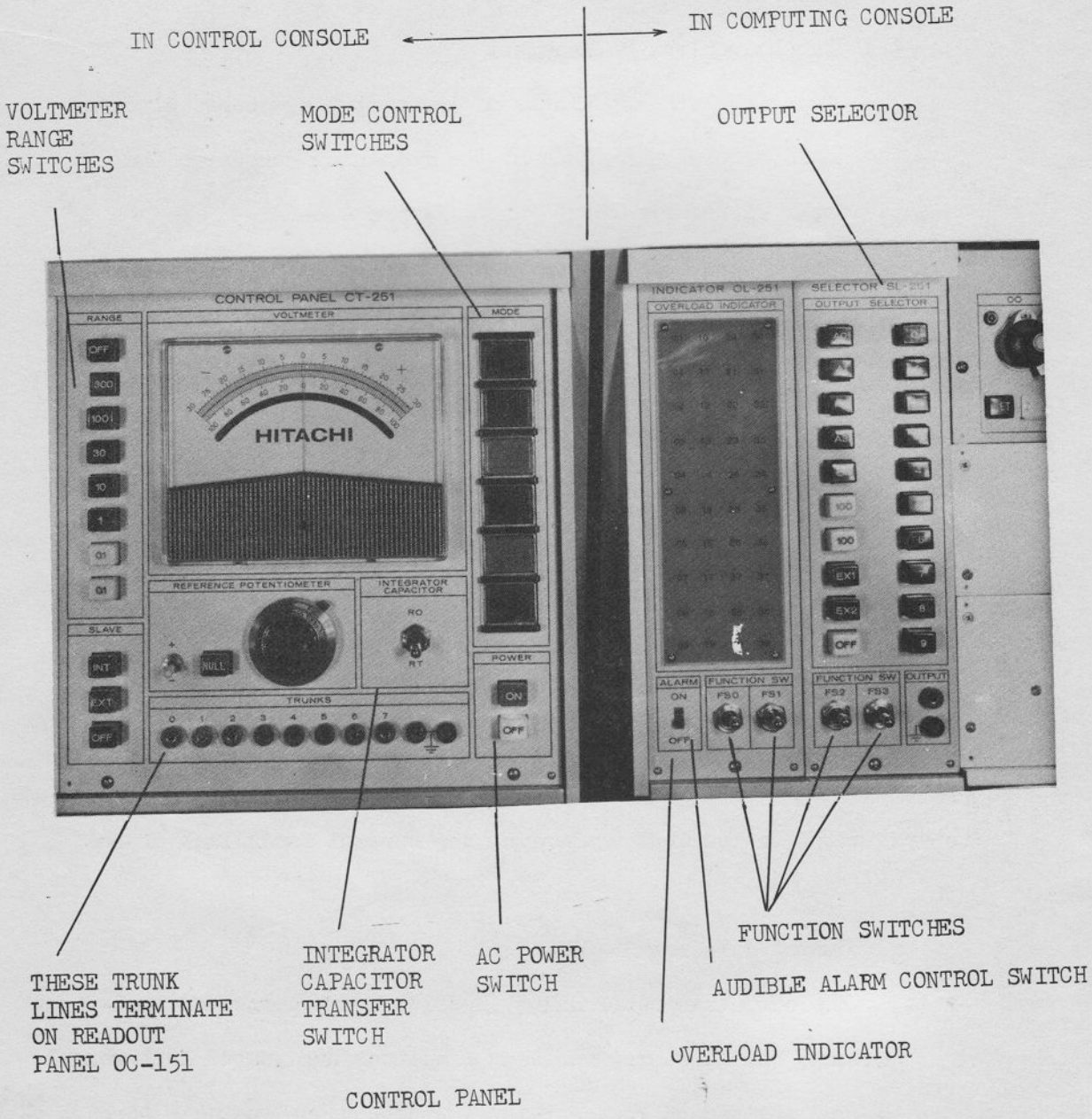


FIGURE 2.3-1 HITACHI 505 CONTROL AREA

the operator to select the outputs of the comparators (ordinally CP0 through CP8).

The two reference voltages are selected only by pushing the buttons designated 100 (red, for positive) or 100 (blue, for negative), nevertheless any button of the second row depressed. The button designated EX1 permit the operator to call an external signal from an external device, for instance the output selector in the additional computing console CS-505A. A button designated EX2 has no connection and is provided as a spare selector.

Depressing the button, one of A0 through A3, sets the selector system for amplifiers in a given tens group, i.e., if the button designated A1 is depressed, amplifiers A10 through A19 are set up for selection. The button in the second row designates which of these ten amplifiers is actually selected. The selector system button numbering corresponds with the amplifier and comparator designations as marked on the Pre-Patch Panel respectively.

The selector system output is connected to the ten terminations marked SEL in the upper portion of the Readout Panel OC-151 (Figure 2.3-1)

In order to read out a selected signal on the DVM, the left bottle plug shown in Figure 2.2-2 must be in place. The multi-range voltmeter (VM) may also be connected to the selector line by installing the correct bottle plug shown in the illustration. It should be noted, however, that the VM circuit will load the output of the selected component with a relatively low impedance and should not be used if the circuit cannot tolerate this load. If the operator requires setting the potentiometer or reading the voltage

accurately, use the voltmeter as a nullmeter utilizing the reference potentiometer as a standard voltage divider.

b. Overload Indicator OL-251

The overload indicators (Figure 2.3-1) provide a visual alarm when an overload occurs in any of the operational amplifiers, i.e., when the summing junction is not at virtual ground. An overload may be due to improper scaling, improper patching or loading.

When the computer is initially turned on, all the indicator lamps may light; however, in a few seconds, as the amplifiers settle, all the lamps should go out. Should a lamp remain lit it could be a patching error such as the failure to provide un-used amplifiers with feed-back (via the four or six connector bottle plugs). Prolonged overload will not damage an amplifier.

To eliminate the audible signal in the initial overload, it is recommended to turn off the switch designated ALARM on the panel.

c. Digital Voltmeter DV-251

The digital voltmeter (DVM) DV-251 is terminated in the Readout Panel OC-151 area (Figure 2.3-2) and is designated DV. As previously mentioned the DV may be bottled to the SEL termination to monitor the selector system voltages, or with a patch cord the digital voltmeter may be used to monitor signal levels at practically any termination in the Pre-Patch Panel. The DVM has a 50 megohm (minimum) full-time input impedance.

It will take about 30 minute warm up time to operate the digital voltmeter in the specified accuracy for the measurement of an absolute voltage. For the analog computer, it is not necessary to obtain the absolute voltage, so the operator may use the digital voltmeter

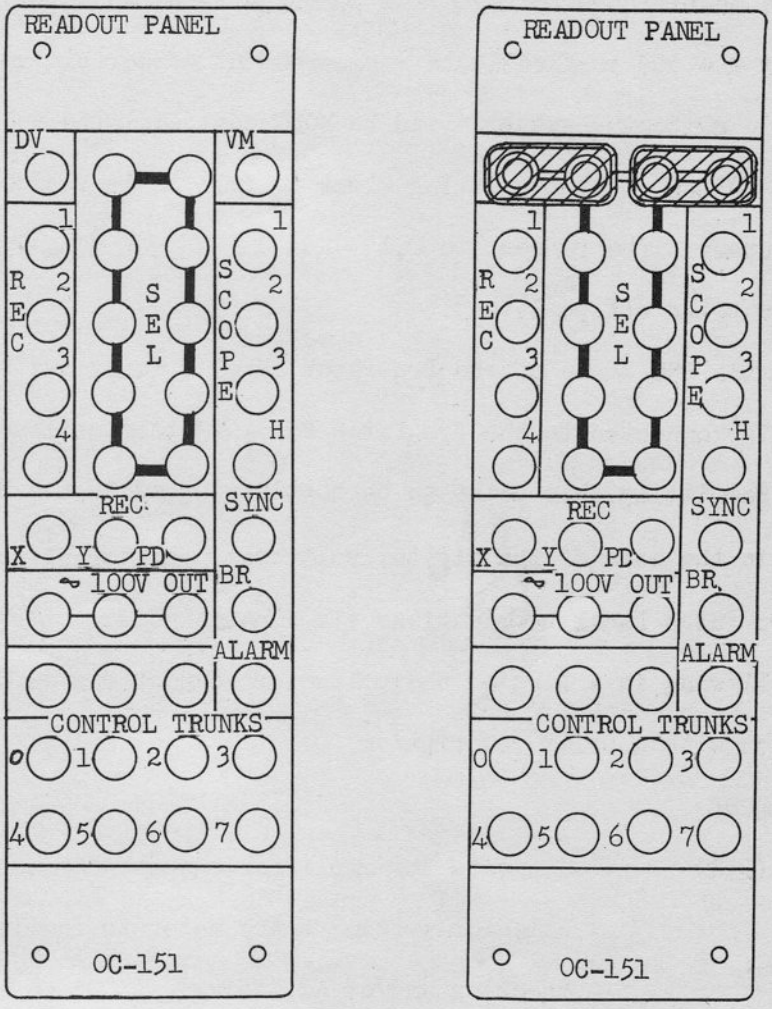


FIGURE 2.3-2 READOUT PANEL OC-151 PATCHING BLOCK AND DVM/VM TO SEL PATCHING

approximately 10 minutes after the power has been switched on.

(d) Multi-Range Voltmeter (in Control Panel CT-251)

The multi-range voltmeter is permanently wired into various circuits of the 505 to facilitate rapid readout of certain voltages by automatic switching synchronized to MODE control. The voltmeter has a RANGE switch, thus permitting close to full scale readouts for maximum accuracy. The ranges are 0.1, -0.1, 1, 10, 30, 100 and 300 volts (in addition to an off position).

In the ENG state of the Pre-Patch Panel driving switch, the RANGE switch is connected to the Pre-Patch Panel VM termination (Figure 2.3-2) permitting this point to be bottle-plugged to the SEL output or, as in the case of the digital voltmeter, monitoring voltages at most Pre-Patch Panel terminations via a patch cord.

Following is a list of the voltmeter connections in each mode of operation with a brief description.

MODE	DESCRIPTION
BC (DIS)	Connects the amplifier output addressed by the selector system to the meter to facilitate checking and/or adjusting. The amplifier balance, notwithstanding the connection on the Pre-Patch Panel.
All modes except BC	Connects the meter to the VM Pre-Patch termination.

In each mode, the connection will be made via the RANGE switch.

If the NULL button in the REFERENCE POTENTIOMETER area is depressed, the voltmeter system with the RANGE switch can be used as a null meter referred to the reference potentiometer. The polarity of the reference voltage (plus or minus 100 volts) which will be applied to the reference potentiometer as a null meter may be decided by the toggle switch next to the NULL push button.

e. Reference Potentiometer (in Control Panel CT-251)

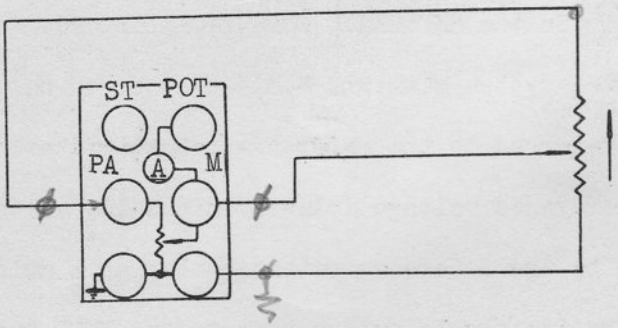
The reference poteniometer on the control panel may be used in two ways; as an ordinary potentiometer and a null meter mentioned already.

In the state that the NULL button is not depressed, the reference potentiometer may be used as an ordinary potentiometer terminated on the FUNCTION SW area of the Pre-Patch Panel (Figure 2.3-3).

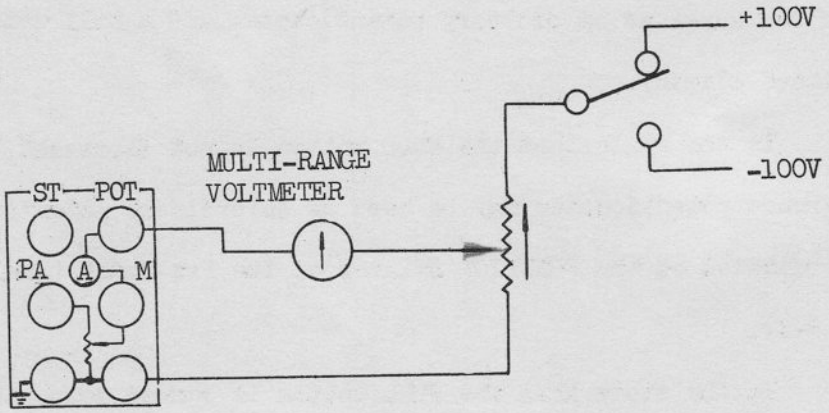
In the state that the NULL button is pushed down, the reference potentiometer may be used as arms of the null meter. In this state, the reference voltage may be applied directly to the top end of the reference potentiometer. The polarity of the voltage is controlled by the toggle switch next to the NULL push button.

f. Mode Control (in control Panel CT-251)

The operating mode of the computer is controlled by the six pushbutton selector just to the above of the POWER button (Figure 2.3-1). Following is a list of the pushbutton and brief description of their functions.



(a) ORDINARY POTENTIOMETER CONNECTION
(THE STATE NULL BUTTON UP)



(b) NULLMETER SYSTEM CONNECTION
(THE STATE NULL BUTTON DOWN)

FIGURE 2.3-3 SIMPLIFIED SCHEMATIC OF REFERENCE POTENTIOMETER

MODE BUTTON	DESCRIPTION
RESET	In the RESET mode all circuits except the integrators function normally. The integrator outputs are held at their respective initial conditions (IC) as dictated by the IC input voltage. (The integrator output is zero if no IC voltage is applied)
COMPUTE	When this pushbutton is depressed, all integrators are simultaneously released to respond to input signal voltages. The integrator outputs change in potential as dictated by the inputs; a time varying behavior is produced. This generates the voltage solution of the programmed problem.
HOLD	Depressing the HOLD pushbutton permits the problem solution to be halted and all voltages held at the potential attained up to the instant of depressing the button. The problem may be continued from this point by depressing the COMPUTE button or re-set to the starting point by depressing the RESET button.

MODE BUTTON	DESCRIPTION
POT SET	Amplifier input resistor summing junction grounded; permits setting potentiometers under actual load. Also provides amplifiers with relay-contact feedback in order that Panel may be removed to balance amplifiers.
ALL RESET	In the ALL RESET mode all circuits except integrators function normally. All integrator outputs are held at their respective initial conditions (IC), regardless the connection of the Integrator driving circuits. This mode may be used especially in separate mode control operation.
REP OP	The REP OP button switches the computer into the repetitive operation mode if the oscilloscope OS-251 or the timer (TM-251 or TM-253) is provided in the 505. In this mode the each of the integrator capacitor will change to the capacitor connected to the terminal designated RO on the integrator area of the Pre-Patch Panel, if the INTEGRATOR CAPACITOR switch on the control panel is located on RO position. If the switch is turned to the RT position, the integrator capacitor connection remains at the terminal designated RT on the integrator area of the Pre-Patch Panel. The latter state will be very useful to operate the

MODE BUTTON	DISCRIPTION
REP OP (Continued)	computer in low speed (Real Time) repetitive or iterative computation. The following table shows the operation in each state simply.

MODE BUTTON	INTEGRATOR CAPACITOR SWITCH	ACTUAL INTEGRATOR CAPACITOR CONNECTION
REP OP	RO	RO
	RT	RT
EXCEPT REP OP	RO	RT
	RT	RT

g. Trunks

There are two types of trunks; Pre-Patch Panel trunks and control trunks. Pre-Patch Panel trunks (terminating at the TRUNKS TR-151 area) provide point-to-point connections to the connectors at the right-rear of the computer (Figure 2.3-4). These connectors may be used as outputs to accessory equipment, or the trunk terminations may be cabled to a second computing console, CS-505A, as signal carrying lines for the interconnection of the problems patched on separate Pre-Patch Panels of slaved computing consoles.

Control trunks (terminating at the Readout Panel OC-151 area) provide point-to-point connections to the Control Panel CT-251. These connectors may be used as input/output channels

.r the temporary connectors to the test equipment.

Slave switches (in Control Panel CT-251)

When a 505 is to be slaved to another 505 (master), the button EXT of the SLAVE area in the Control Panel is depressed. The slaved computer then responds to the selected modes of the master computer pushbuttons.

When a 505 is to be controlled by the Digital Element Panel or the Timer, the button INT of the SLAVE area is depressed. Then, the computer is driven with signals from input of the analog patchboard or the digital patchboard. For normal manual operation, the OFF button of the SLAVE area should be kept down.

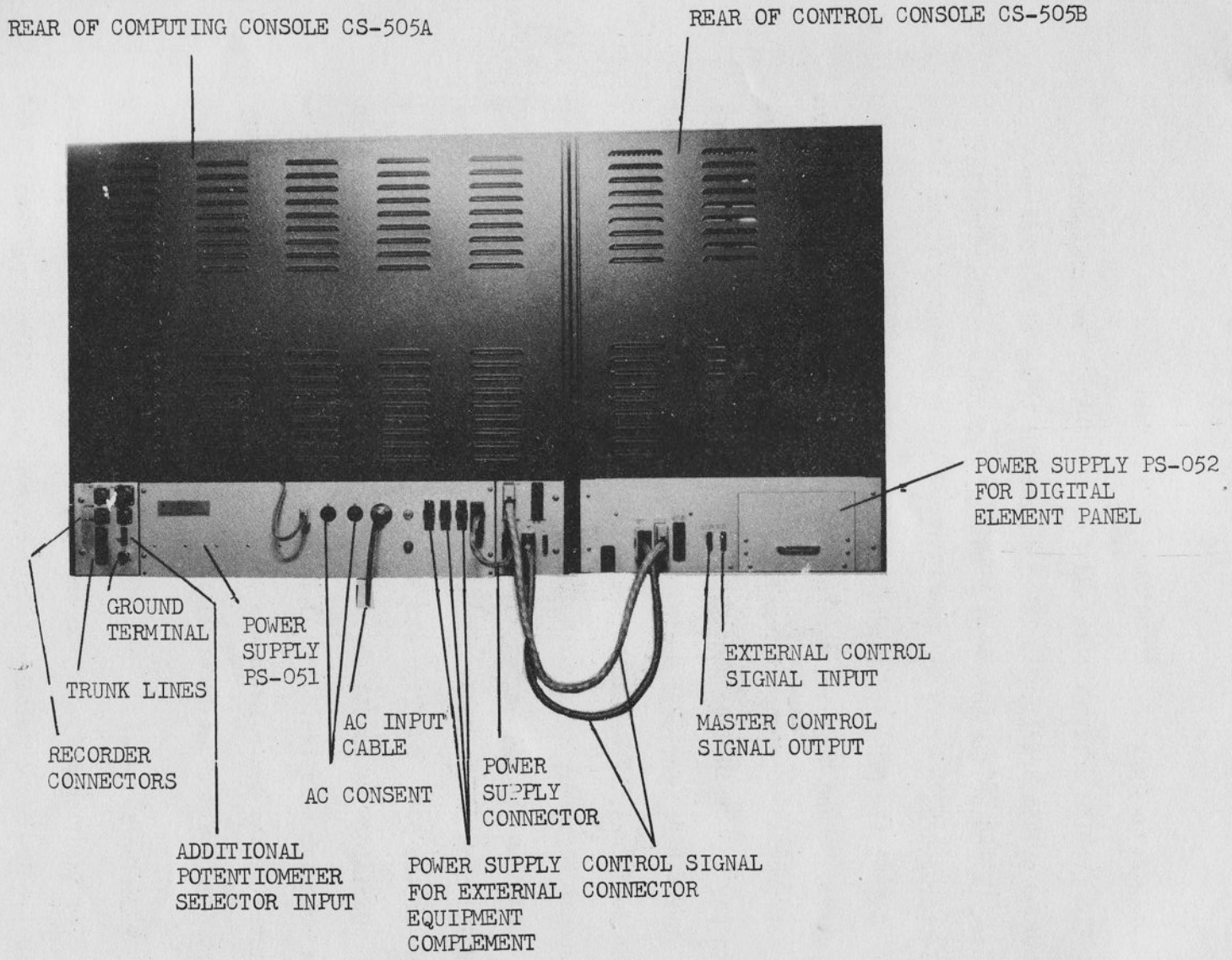


FIGURE 2.3-4 CONNECTING AREA, REAR THE COMPUTING CONSOLE CS-505A

i. Readout Devices

The problem solution obtained from the 505 may be permanently recorded or temporarily displayed on various types of readout devices. A few of the more common readout devices are described in this paragraph.

Either the DVM or voltmeter may be used to read out the problem solution. These devices, however, do not record the solution and thus do not provide a permanent record. When in REP-OP the computer solution may be obtained by photographing the scope trace. X-Y recorders or strip-chart recorders may be used for permanent record of 505 problem solutions. These units, however, do not have the frequency response necessary to accurately record the solution when the computer is placed in the high-speed REP-OP mode of operation. The recorder terminations on the Readout Panel are wired to connector plugs at the rear of the 505. See Figure 2.3-4.

Oscilloscope OS-251 is especially prepared for the exhibition of the computer solution. The OS-251 has three channel inputs and can be mounted on the Control Console CS-505B. All input terminals are connected on the Readout Panel OC-151 area in the Patchboard.

j. Function Switches

The Function Switches (on the Overload Indicator OL-251 and Output Selector SL-251, 4 switches total) provide 3-position single-pole (FS0, FS1) and double-pole(FS2, FS3) contacts. They are terminated on the Function Switch FS-151 area of the patchboard. With these switches the operator may manually switch computer problem functions. The center position may be considered the off position.

k. Power Switches (in Control Panel CT-251)

The AC power to operate the computer is controlled by the POWER switches on the Control Panel CT-251. When the AC cord is connected from an external AC source to the Power Supply, the OFF switch will light and notify the operator that AC power is ready, the Oven in the computing console is working and Pre-Patch Panel driving mechanism is ready to actuate.

When ON switch is pushed, the Power Supply PS-051 will furnish all the DC, AC and square-wave power necessary to operate the whole computer.

4. POTENTIOMETERS

One of the simplest and most useful operations performed on an analog computer is the multiplication of a variable voltage by a ~~signal~~ CONSTANT FACTOR. The Hitachi 505 has a basic complement 18 potentiometers and may be expanded to a full complement of 54 potentiometers.

Each Potentiometer Panel PT-251 provides 18 potentiometers for setting problem coefficients, initial conditions, and problem inputs. The potentiometers are mounted to a maximum of 3 horizontal rows of 18 potentiometers per row. Each row is terminated at a corresponding row of the Pre-Patch Panel; three modules PT-151 of a row in the Pre-Patch Panel terminate a Potentiometer Panel PT-251. Each Potentiometer Patch Module PT-151 contains 6 potentiometer terminals. Five of the six poteniometers have one end grounded while the sixth has both ends ungrounded. (See Figure 2.4-1)

The standard potentiometers in the 505 are 10 turn, wirewound, 30K ohms, individually fused units with calibrated dials and a locking mechanism.

The potentiometer may be used in conjunction with reference to obtain a fixed accurate voltage less than reference, or to multiply a problem variable by any constant less than unity. Figure 2.4-1 is a schematic of a potentiometer with +100 volts applied to the high end*, where K is;

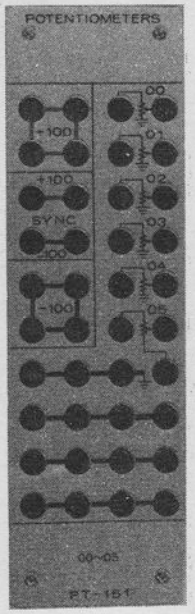
$$K = \frac{R_1}{R_t} \qquad \text{(EQ.2.4-1)}$$

The potentiometer shown in Figure 2.4-5 is unloaded, and the mechanical ratio of $R_1:R_t$ equals the electrical ratio $e_o:e_{in}$; thus, the potentiometer may be set to the exact ratio by means of the calibrated dial attached to the wiper shaft. However, the two ratios will not be equal when the potentiometer is loaded as is the case when it is used as a computer problem element. Normally, the pot is loaded by either a 1M or 100K ohm resistor since a potentiometer generally feeds an amplifier and these values are the most common amplifier input resistors. Figure 2.4-3 illustrates the effect on the $e_{in}:e_o$ and $R_1:R_t$ ratios when the potentiometer wiper feeds a 100K load.

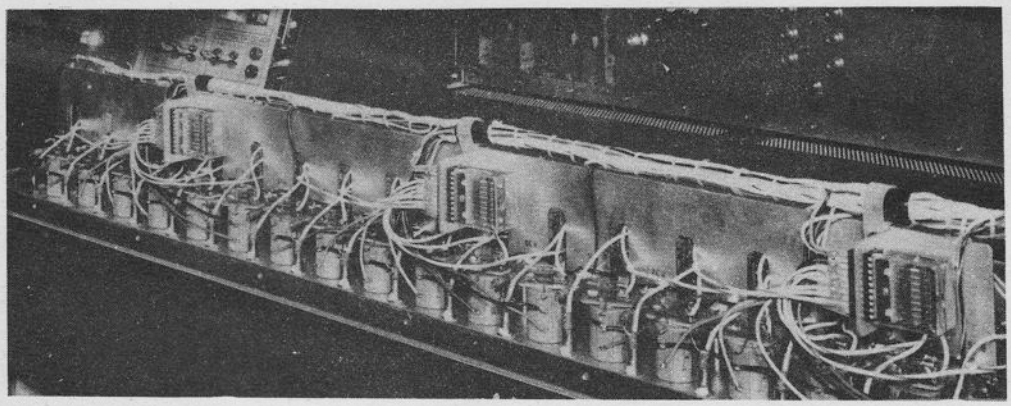
In order to eleminate the effects of loading, it is more convenient to set the poteniometers under actual load and monitor the wiper voltage

---

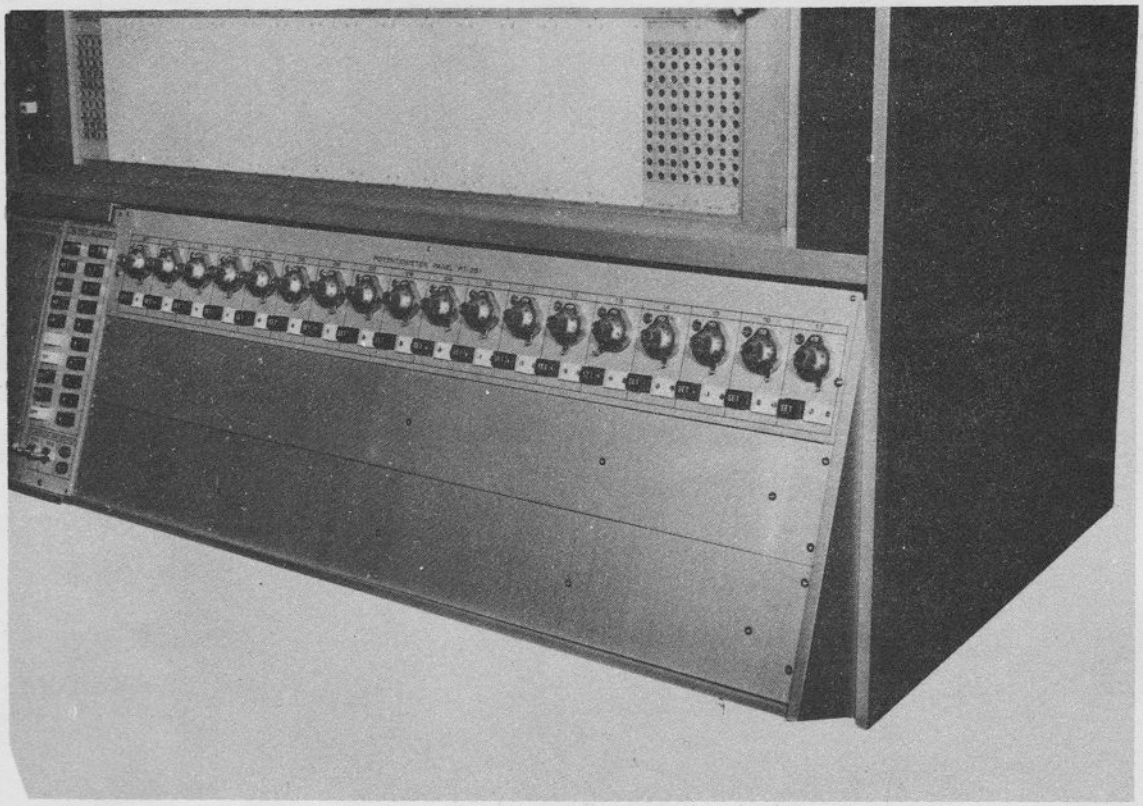
* The high end of a potentiometer refers to the termination of the Pre- located at the top of the schematic designation of the Pre-Patch Panel. The low end is the bottom termination, normally grounded except in the case of the ungrounded potentiometer.



PATCHING UNIT



FUSE LOCATION
(REAR OF POTENTIOMETER PANEL)



POTENTIOMETER PANEL

FIGURE 2.4-1 POTENTIOMETER PATCHING UNIT PT-151
AND POTENTIOMETER PANEL PT-251

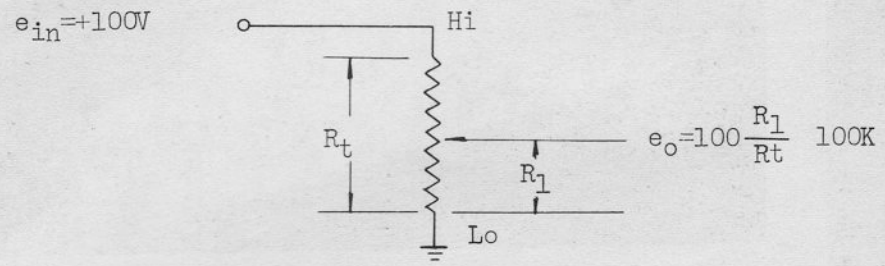
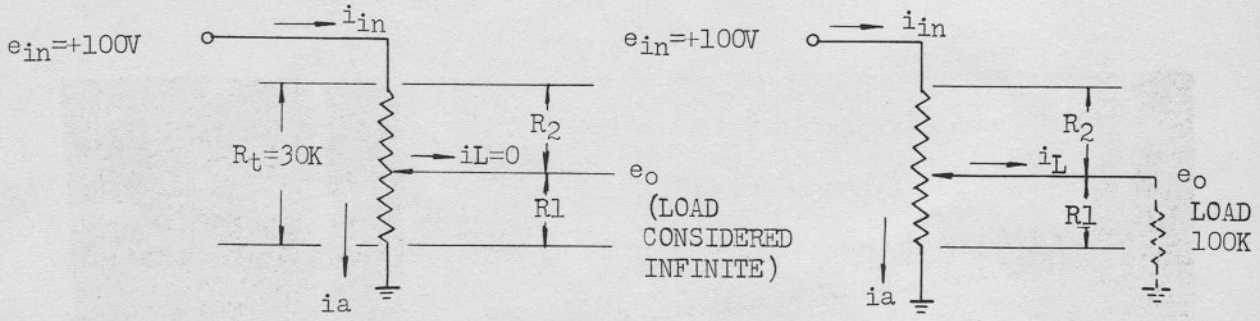


FIGURE 2.4-2 POTENTIOMETER SCHEMATIC SHOWING e_{in} TO e_o RELATIONSHIP FOR e_{in}=100 VOLTS



(a) INFINITE LOAD: DIAL SET AT 0.33 (b) 100K LOAD: DIAL SET AT 0.

(a) INFINITE LOAD: DIAL SET AT 0.833

$\therefore R_1$ =25K R_2=5K

e_o =100-i_{in} R_2

$i_{in}=i_L+i_a$

$i_{in}=i_a$=3.33 ma. i_L=0

$\therefore e_o$ =100-3.33(5)=83.3 VOLTS

$\frac{R_1}{R_t}$=0.833 (AS SET BY DIAL)

$\frac{e_o}{e_{in}}=\frac{83.3}{100}$= 0.833

$\therefore \frac{R_1}{R_t}=\frac{e_o}{e_{in}}$

(b) 100K LOAD: DIAL SET AT 0.833

$\therefore R_1$ =25K R_2=5K

e_o =100-i_{in} R_2

$i_{in}=i_L+i_a$

WITH 100K LOAD i_{in}=4.00 ma.

$\therefore e_o$ =100-4.00(5)=80.0 VOLTS

$\frac{R_1}{R_t} \neq e_o$

FIGURE 2.4-3 POTENTIOMETER LOADING

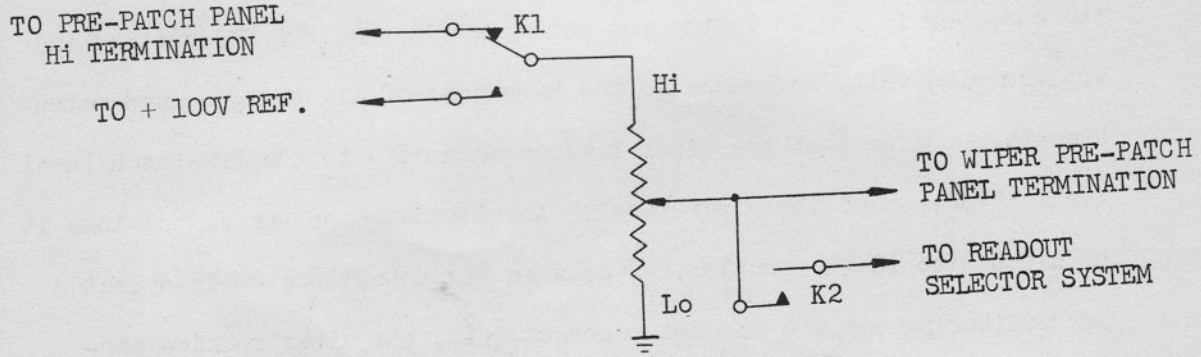
(The potentiometer output), than to calculate a corrected mechanical ratio ($R1:R_t$).

Figure 2.4-4 illustrates the 505 circuitry provided to permit setting the potentiometers under actual load. Relay K1 is energized when the computer is placed in the pot set mode (depress POT SET button) and applies +100 volts reference to the high ends of all the grounded potentiometers. Note that the wiper remains connected to the Pre-Patch Panel termination; thus, the wiper "feels" the impedance of the actual load it is patched to in the problem. Even when the potentiometer is selected for monitoring via the readout pushbutton K1, the wiper remains connected to its actual load. The readout pushbutton connects the wiper to a high impedance DVM or, in the absence of the DVM, a null pot circuit. The operator may then set the wiper for the attenuation factor required in the problem.

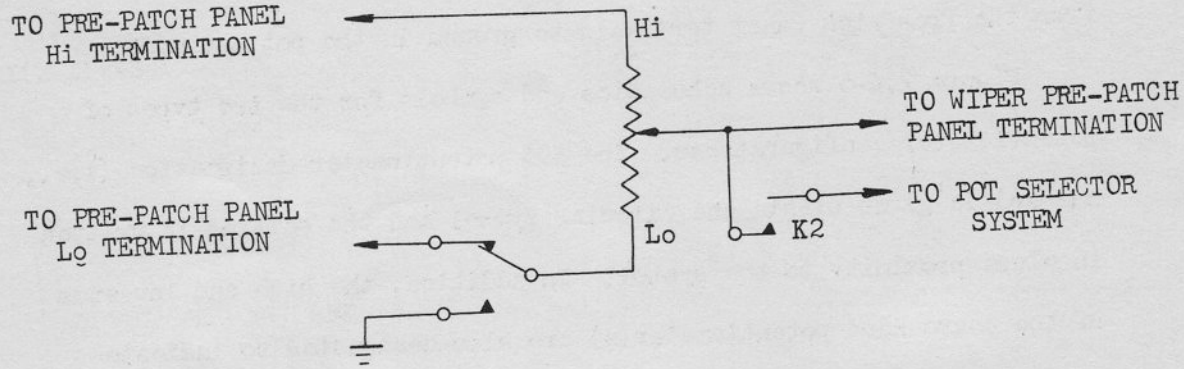
The method of the setting the ungrounded potentiometers is quite similar to the setting the grounded ones. The low ends are transfered from the Pre-Patch Panel terminals to ground in the pot set mode.

Figure 2.4-5 shows schematics and symbols for the two types of potentiometer configurations. The 505 potentiometer designation (i.e., number) is given within the circular symbol and the setting is written in close proximity to the symbol. In addition, the high and low ends of the ungrounded potentiometer(s) are also designated to indicate clearly both input signal sources.

The neon lamp located at the left side of the each potentiometer will light when the potentiometer readout button just below the potentiometer is pushed, and notify the operator that this potentiometer connected to the readout system.

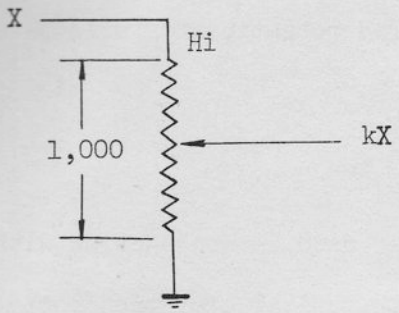


a. GROUNDED POTENTIOMETER CIRCUIT

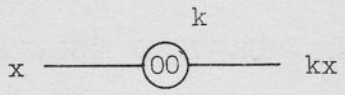


b. UNGROUNDED POTENTIOMETER CIRCUIT

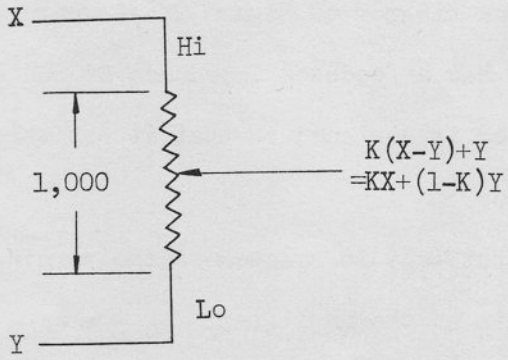
FIGURE 2.4-4 505 POTENTIOMETER CIRCUITS, SIMPLIFIED SHEMATIC



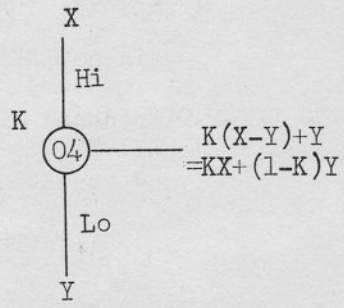
a. GROUNDED POT SCHEMATIC



b. GROUNDED POT COMPUTER DIAGRAM SYMBOL



c. UNGROUNDED POT SCHEMATIC



d. UNGROUNDED POT COMPUTER DIAGRAM SYMBOL

NOTE: $K=e_o/e_{in}$

FIGURE 2.4-5 POTENTIOMETER SCHEMATIC AND COMPUTER SYMBOLS

The potentiometer having a lower number has priority. When two buttons are pushed, the lower numbered potentiometer will be selected.

5. OPERATIONAL AMPLIFIER

a. General Considerations

When a high-gain d-c amplifier is used in conjunction with input and feedback networks to perform mathematical operations, the resulting system is generally referred to as an operational amplfier. The operational amplifier is the basic and most versatile unit in the analog computer. It can be used for inversion, summation, multiplication by a constant, integration, and used in conjunction with special networks for squaring, extracting square root, generating logarithmic functions, etc.

To understand the basic concept of the operational amplifier, consider the simplified block diagram of Figure 2.5-1 where a high-gain amplifier (gain of -A) has a feedback impedance Z_f and an input impedance Zin. The amplifier is designed so that it has three basic and essential characteristics.

(1) The amplifier output (e_o) is related to the summing junction voltage (e_s) by the gain of the amplifier: $e_o = -Ae_s$

(2) The input stage of the amplifier draws neglisible current: $i_b \approx 0$

(3) The open loop gain of the amplifier is extremely high: $A \gg 1$ (on the order of 10^7 at d-c).

Using Kirchhoff's laws, the nodal current equation at the summing junction (SJ) is:

$$i_{in} = i_f + i_b$$

or

$$\frac{e_{in} - e_s}{Z_{in}} = \frac{e_s - e_o}{Z_f} + i_b \qquad \text{(EQ. 2.5-1)}$$

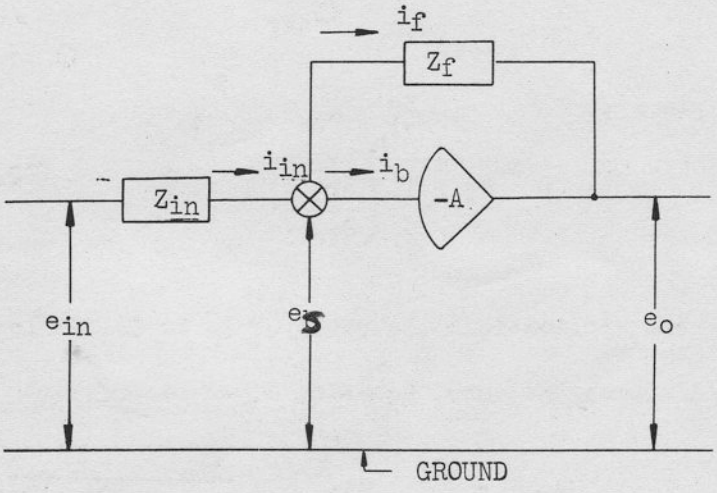


FIGURE 2.5-1 OPERATIONAL AMPLIFIER, SIMPLIFIED BLOCK DIAGRAM

since $e_s = e_o/A$, and since $i_b \approx 0$, Equation 2.5-1 can be rewritten to obtain:

$$\frac{e_{in}}{Z_{in}} + \frac{e_o}{AZ_{in}} = -\frac{e_o}{AZ_f} - \frac{e_o}{Z_f}$$

Solving for e_o:

$$e_o = \frac{-\frac{Z_f}{Z_{in}} e_{in}}{1 + \frac{1}{A}\left[\frac{Z_f}{Z_{in}} + 1\right]} \qquad \text{(EQ. 2.5-2)}$$

In most applications the ratio of Z_f to Z_{in} is less than 30 and since 1/A approaches zero, Equation 2.5-2 becomes:

$$e_o = -\frac{Z_f}{Z_{in}} e_{in} \qquad \text{(EQ. 2.5-3)}$$

Equation 2.5-3 illustrates one of the most important considerations of the operational amplifier: The input output relationship of the operational amplifier is solely dependent on the ratio of the feedback to the input impedance.

Using Equation 2.5-3 as the basis of discussion, the following subparagraphs describe the various uses of the operational amplifier.

(1) Inversion

When the same value resistor is used for both the feedback and the input impedance, the amplifier output voltage has the same amplitude as the input voltage but is opposite in polarity.

$$e_o = -\frac{R_f}{R_{in}} e_{in}$$

In the 505, the value of R_f and R_i used for the inverter is normally 1M ohms, therefore:

$$e_o = - \frac{1M}{1M} \; e_{in} = -e_{in}$$

Thus a +100 volt input results in a -100 volt output, and the amplifier is said to have a gain of minus one. The accuracy of the output to input ratio depends solely on the accuracy of the ratio R_f/R_{in}.

(2) Multiplication by a Constant A change in the ratio of the resistors results in multiplication by a constant. With R_f equal to 1M and R_{in} equal to 100K for example, the amplifier output is:

$$e_o = - \frac{1M}{100K} \; e_{in} = -10 \; e_{in}$$

An input of plus 10 volts results in an output of minus a hundred volts. This operational amplifier has a gain of ten. The multiplying constant can be made less than one by using a 100K feedback resistor with a 1M input resistor.

$$e_o = - \frac{100K}{1M} \; e_{in} = -0.1 \; e_{in}$$

An input of minus 100 volts produces an output of 10 volts.

(3) Summation When multiple input resistors are used with a feedback resistor R_f, the basic relationship is extended to:

$$e_o = - \left(\frac{R_f}{R_1} e_1 + \frac{R_f}{R_2} e_2 + \ldots + \frac{R_f}{R_n} e_n \right)$$

The circuit can be used to algebraically sum an indefinite number of inputs; furthermore, each input may be multiplied by an arbitrary constant.

(4) Integration with Respect to Time When the feedback element Zf is a capacitor rather than a resistor the summing junction current equation is;

$$\frac{e_1}{R_1} + \frac{e_2}{R_2} + \ldots + \frac{e_n}{R_n} = -C\frac{de_o}{dt}$$

Integrating this equation and assuming an initial charge on the feedback capacitor of Vo:

$$e_o = -\frac{1}{C}\int_o^t \left(\frac{e_1}{R_1} + \frac{e_2}{R_2} + \ldots + \frac{e_n}{R_n}\right)dt + Vo$$

Looking at this another way, if Zf is a capacitor having an operational impedance $1/pC$ and Z_{in} is a resistor, the basic operational amplifier relationship, Equation 2.5-3 becomes

$$e_o = -\frac{E_{in}}{pRC} = -\frac{1}{RC}\int_o^t e_{in}dt$$

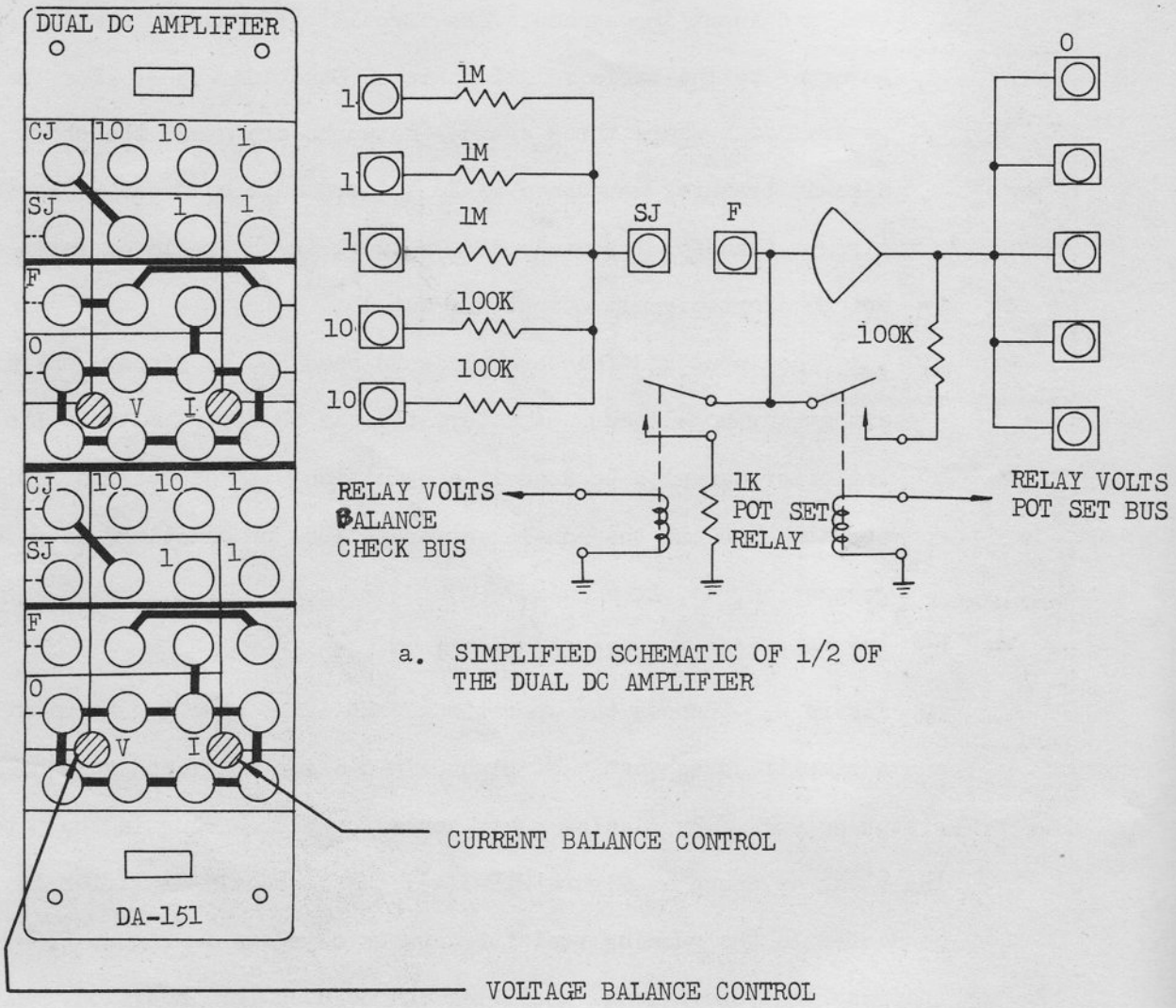
With this arrangement, the operational amplifier will integrate (with respect to time) any input voltage. In addition to integrating, the amplifier also inverts the input voltage. An indefinite number of input may be applied to produce the time integral of the sum of the input voltages.

(5) Other Mathematical Operations As previously indicated the operational amplifier has uses other than those indicated in sub-paragraph (1) through (2). Complicated transfer functions can be simulated by using series and parallel RC networks for the feedback and input impedances. The circuit performance is still governed by the basic relationship of Equation 2.5-3. For the general case where three channel networks are used, the short circuit transfer impedance of Z_f and Z_{in} must be used. (The short circuit transfer impedance of a network is the ratio of input voltage to short-circuit output current.)

The input and feedback elements need not be linear; therefore, almost any non-linear characteristic can be approximated. The amplifier can also be used in conjunction with diodes and resistors to simulate the non-linear operations of limiting, dead-zone generation, X^2, LogX, etc.

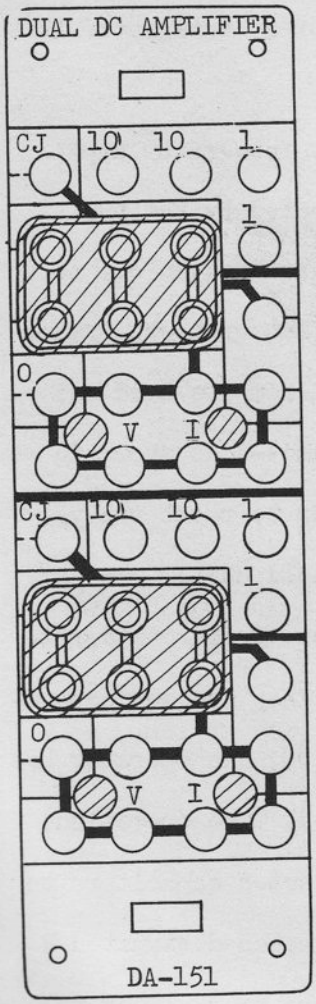
b. 505 Operational Amplifier DA-151

Figure 2.5-2 shows the operational amplifier patching terminations and a simplified schematic of high gain d-c amplifier and summing resistor network. By placing a six connector bottle plug in the patching block as shown in Figure 2.5-3(a), the high-gain amplifier is connected to the summing resistor network as shown in Figure 2.5-3(b). The resultant operational amplifier can be used for inversion, multiplication by a constant, and summation. The computer diagram symbol is shown in Figure 2.5-3(c). On the computer diagram it is customary to shown only those inputs that are used; the amplifier number is written inside the triangular symbol.

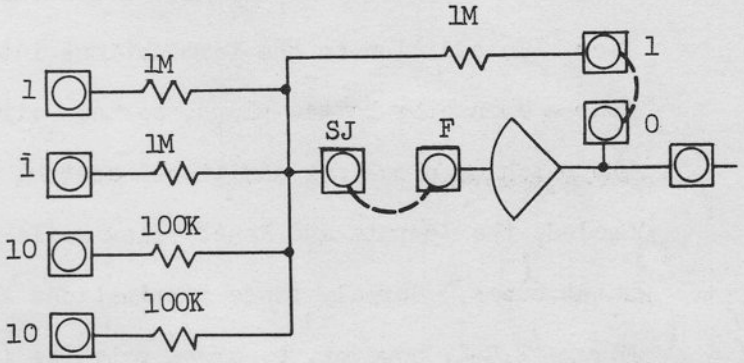


a. SIMPLIFIED SCHEMATIC OF 1/2 OF THE DUAL DC AMPLIFIER

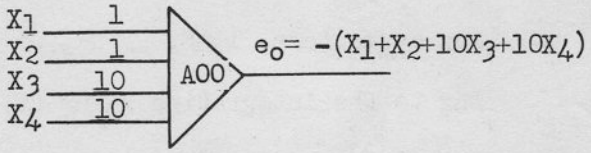
FIGURE 2.5-2 OPERATIONAL AMPLIFIER, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK LAYOUT



(a)



(b)



(c)

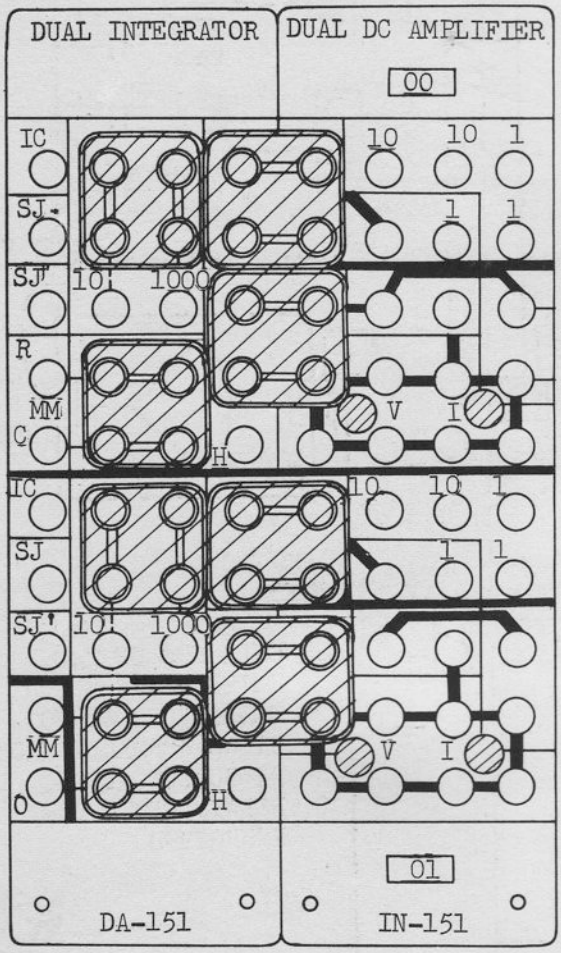
NOTE: IF AMPLIFIER IS NOT USED, BOTTLE PLUG REQUIRED TO PROVIDE FEEDBACK.

FIGURE 2.5-3 SUMMER AMPLIFIER PATCHING

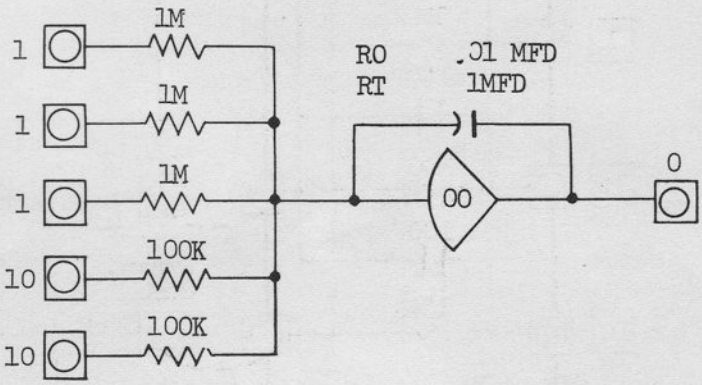
Figure 2.5-4(a) shows the patching to provide an operational amplifier that is capable of integrating with respect to time. Figure 2.5-4(b) illustrates a simplified schematic for an amplifier patched as an integrator. The computer symbol for an integrator is shown in Figure 2.5-4(c).

Figure 2.5-5 is an expanded schematic of the integrator amplifier. In addition to the terminations interconnected by the two four - connector bottle plugs, certain circuits are brought out to the patching block for additional control of the integrators. These include the Compute and Reset relay coils and the compute hold and reset buses. Normaly these terminations are connected as shown in Figure 2.5-4; however, by cross patching (hold bus to reset relay, etc.) the integrator can be used as a track and hold unit.

An additional feature is the free termination of four integrating capacitors; 1 uF, .1 uF,.01 uF and .001 uF. They are corresponding to the integrating gains of 1, 10, 100 and 1000. the operator has the choice of the integrating gain both in RT (real time operation) and RO (repetitive operation), connecting the selected capacitors to RT and RO terminals on the patch panel. The two holes designated R and C of the MM area of the Dual Integrator are the trunk lines to control the integrator mode by the digital logic elements which will be mounted on the Control Console CS-505B.

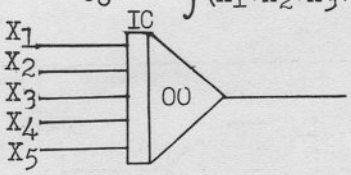


a. INTEGRATOR PATCHING



b. INTEGRATOR SIMPLIFIED SCHEMATIC

$$e_o = -\int (X_1+X_2+X_3+10X_4+10X_5)dt - IC$$



c. COMPUTER DIAGRAM SYMBOLS

NOTE: IF AMPLIFIER IS NOT USED, BOTTLE PLUG REQUIRED TO PROVIDE FEEDBACK.

FIGURE 2.5-4 INTEGRATOR PATCHING AND DIAGRAM

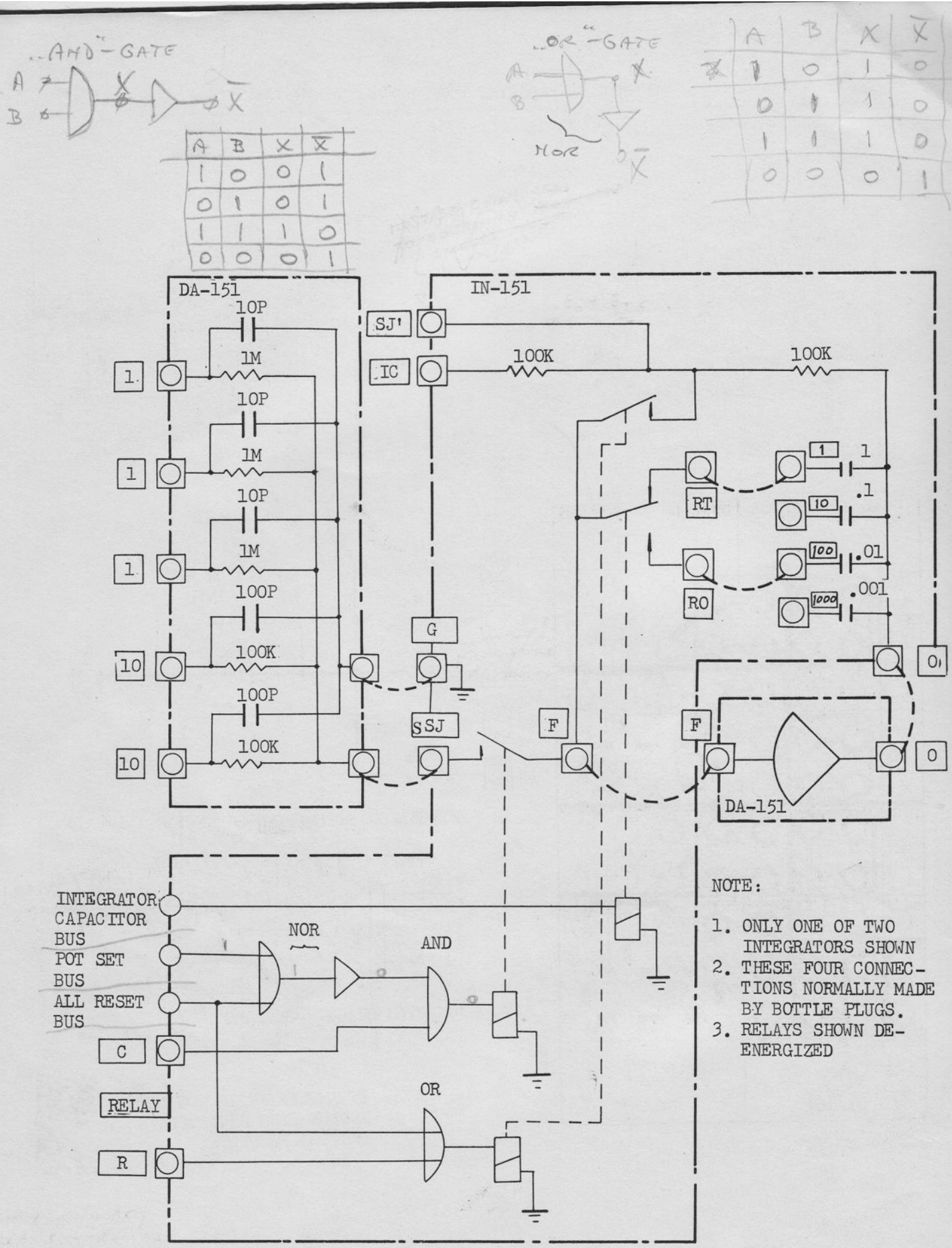
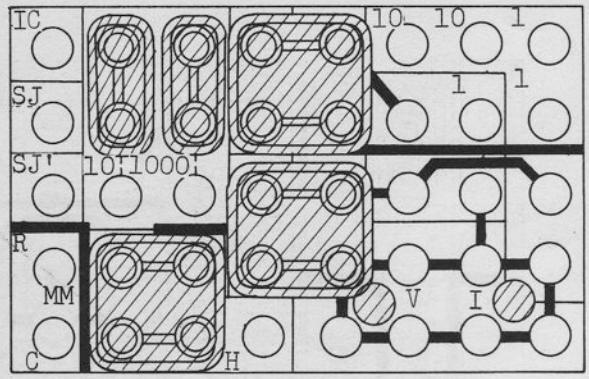


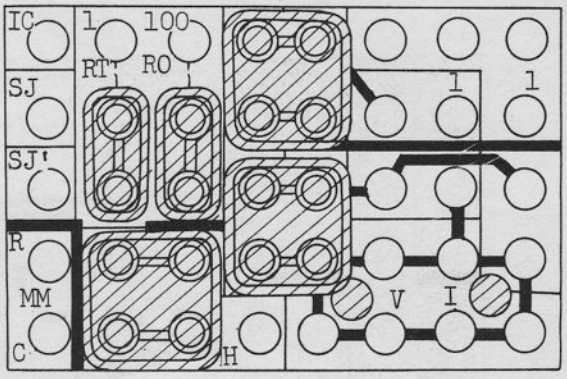
FIGURE 2.5-5 INTEGRATOR AMPLIFIER AND SIMPLIFIED SCHEMATIC

1. ORDINARY OPERATION (1)



INTEGRATING GAIN RT: 1

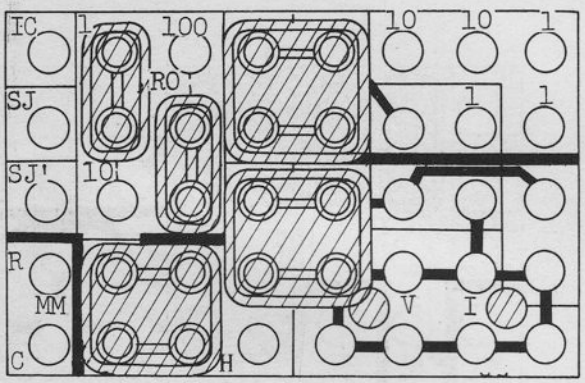
RO: 100



INTEGRATING GAIN RT: 10

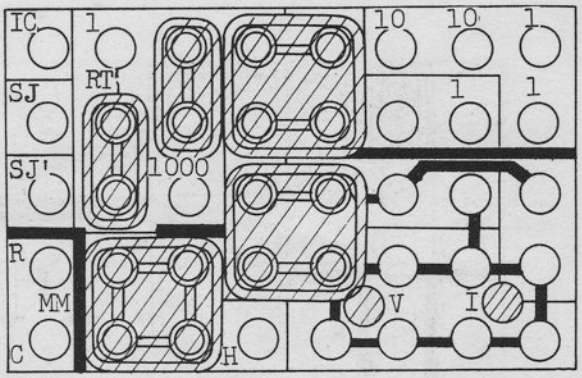
RO: 1000

2. ORDINARY OPERATION (2)



INTEGRATING GAIN RT: 1

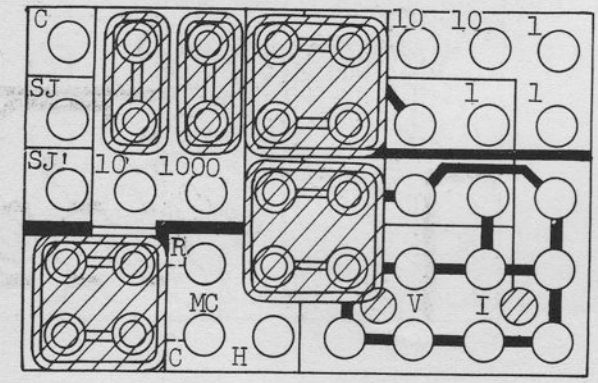
RO: 1000



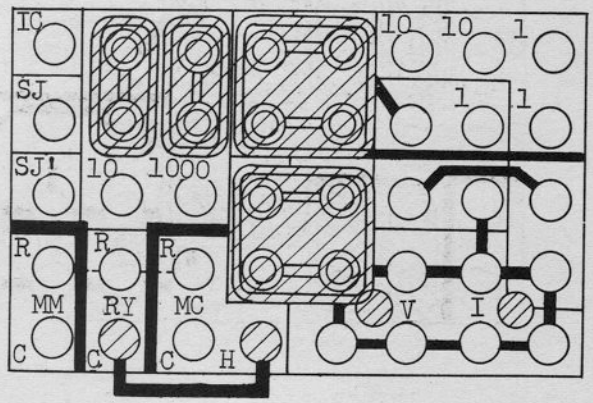
INTEGRATING GAIN RT: 10

RO: 100

3. SPECIAL OPERATION (1)



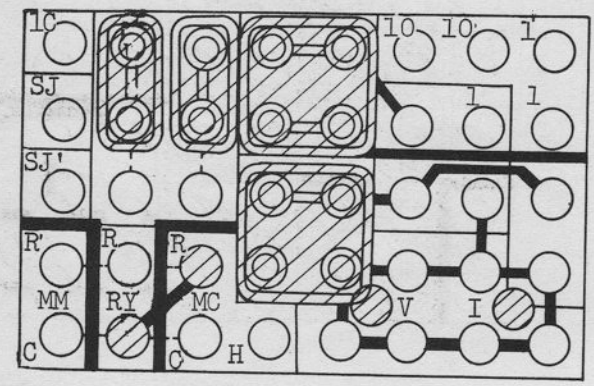
MODE CONTROL BY MODE MATRIX
IN DIGITAL LOGIC AREA



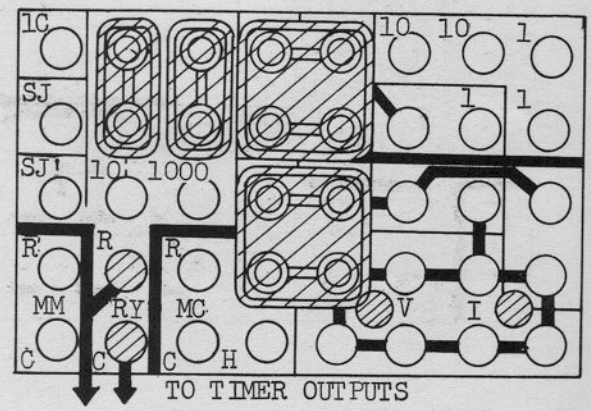
THE INTEGRATOR COMPUTES IN

HOLD MODE

4. SPECIAL OPERATION (2)



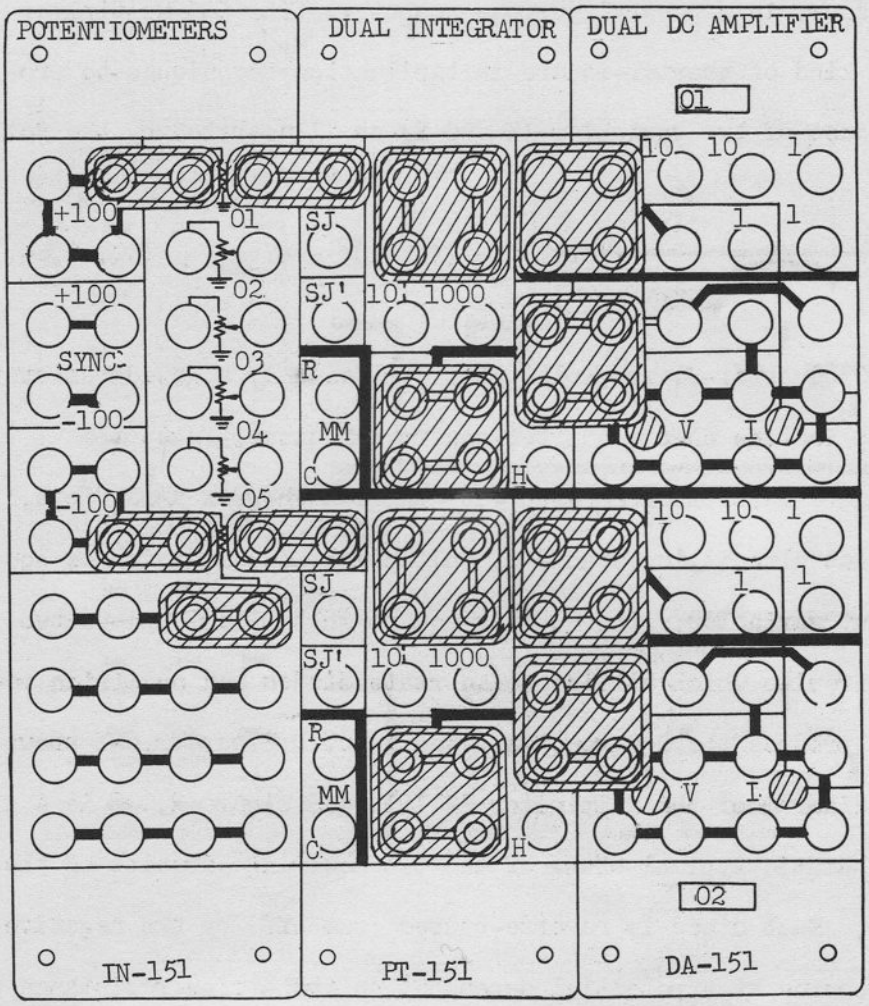
THE INTEGRATOR COMPUTERS
IN RESET MODE



THE INTEGRATOR IS CONTROLLED

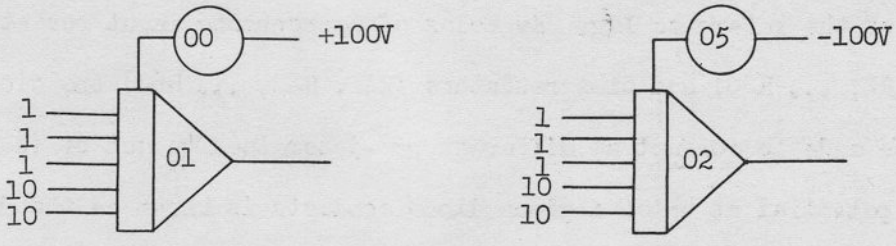
BY THE TIMER.

5. TYPICAL CONNECTION AROUND IN-151



THE PATCHING SHOWS TWO ORDINARY INTEGRATORS

HAVING THE CIRCUITS BELOW.



IN REP OP MODE INTEGRATING GAIN IS MULTIPLIED BY 100.

6. QUARTER-SQUARE MULTIPLIER EM-151

Multiplication of two variables is one of the non-linear operations necessary in a general purpose computer. The 505 Multiplier utilizes a kind of quarter-square multiplication techniques to produce a product of two variables (X and Y) as illustrated by the following equation:

$$XY = \frac{1}{4}\left[(X+Y+1)^2 - (X-Y+1)^2 - 4Y\right] \qquad \text{(EQ. 2.6-1)}$$

The 505 Quarter-Square Multiplier is basically a gated-resistor circuit application of the quarter-square technique. When the quarter-square multiplier is used with three high-gain amplifiers, the resultant circuit is capable of multiplication, division or squaring of input variables. The quarter-square multiplier employs two squaring circuits which utilize solid state diodes and precision resistors to produce the square of a given input. Figure 2.6-1 shows the block diagram of the Multiplier EM-151, and Figure 2.6-2 is a simplified schematic typical of one of the two squaring circuits of the multiplier. Each diode is reverse-biased (cut off) by the negative reference source at a potential dependent on the series resistance (R41, R42 ... R60) in the reference source leg. To cause a given diode to conduct, the sum of the X and Y input (applied via the summing amplifier) must attain a potential opposite in polarity and larger than the bias of the reference leg. By means of appropriate input resistors (R1, R2, ... R20) and bias resistors (R41, R42, ... R60) the diodes may be made to conduct at different pre-determined values of (X+Y). (The potential at which a given diode conducts is known as the diode breakpoint).

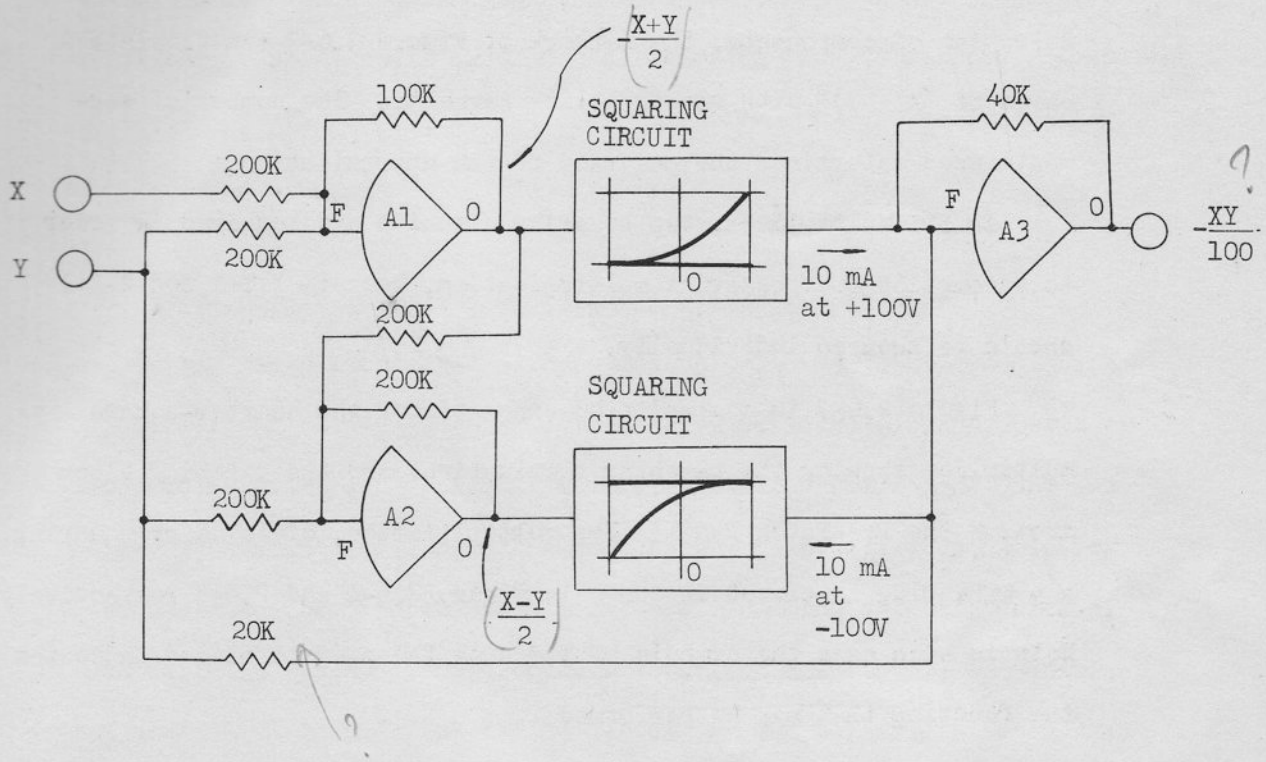


FIGURE 2.6-1 MULTIPLIER, SIMPLIFIED BLOCK DIAGRAM

As the input (X + Y) reaches the breakpoint of each diode, the input resistors are essentially paralleled. The gain of the operational amplifier changes as each diode conducts; therefore, by proper selection of components, the network of Figure 2.6-2 can simulate a curve of $(X + Y)^2$ with straight-line segments. The number of segments used determines the accuracy of the approximation.

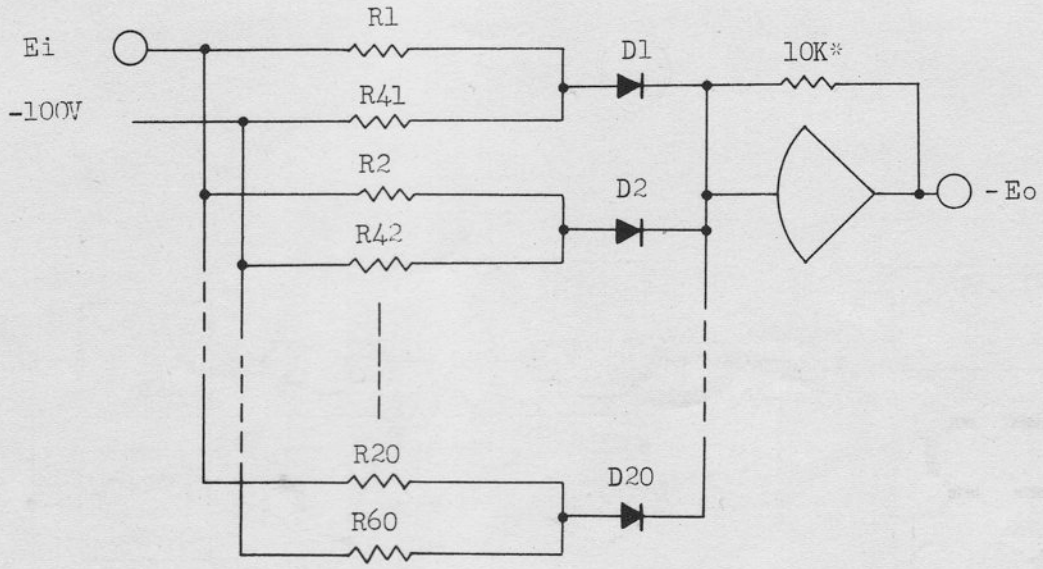
In 505 Multipliers, two squaring circuits are required in order to accomplish four quadrant multiplication, because X+Y+1 and X-Y+1 should be squared individually.

Figure 2.6-3 is a simplified schematic of the quarter-square multiplier showing the patching terminations and the patching block area of the Pre-Patch Panel. For multiplication, division or squaring, a bottle plug is placed as shown in Figure 2.6-4 and 2.6-5 respectively. Note in each case the symbols of the area the plug to placed indicates the function that may be performed.

a. Multiplication

Figure 2.6-4 illustrates the patching procedure for multiplication of two variables, X and Y. Two inputs (X and Y) are necessary notwithstanding the polarity.

Note that the output voltage from the third amplifier is -XY/100 due to the inversion of the amplifier.



* 40K IN MULTIPLIER

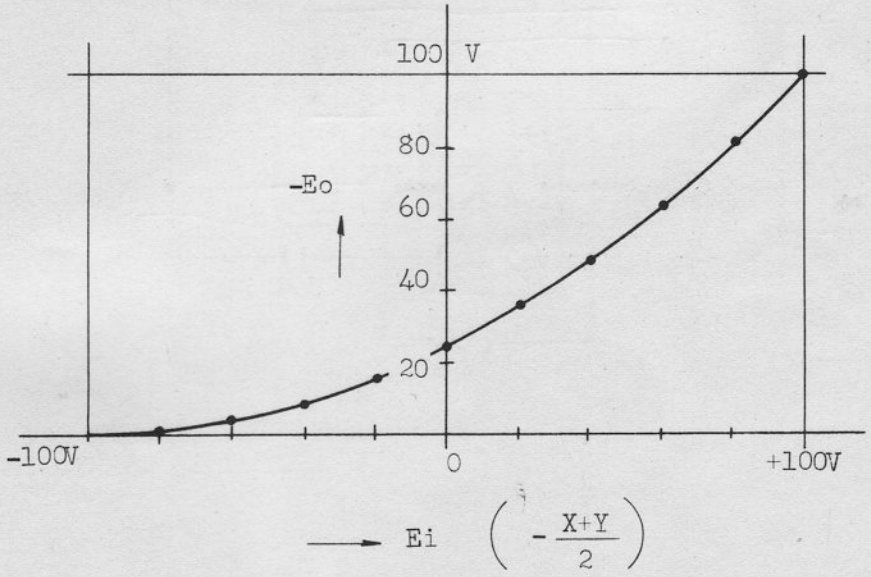
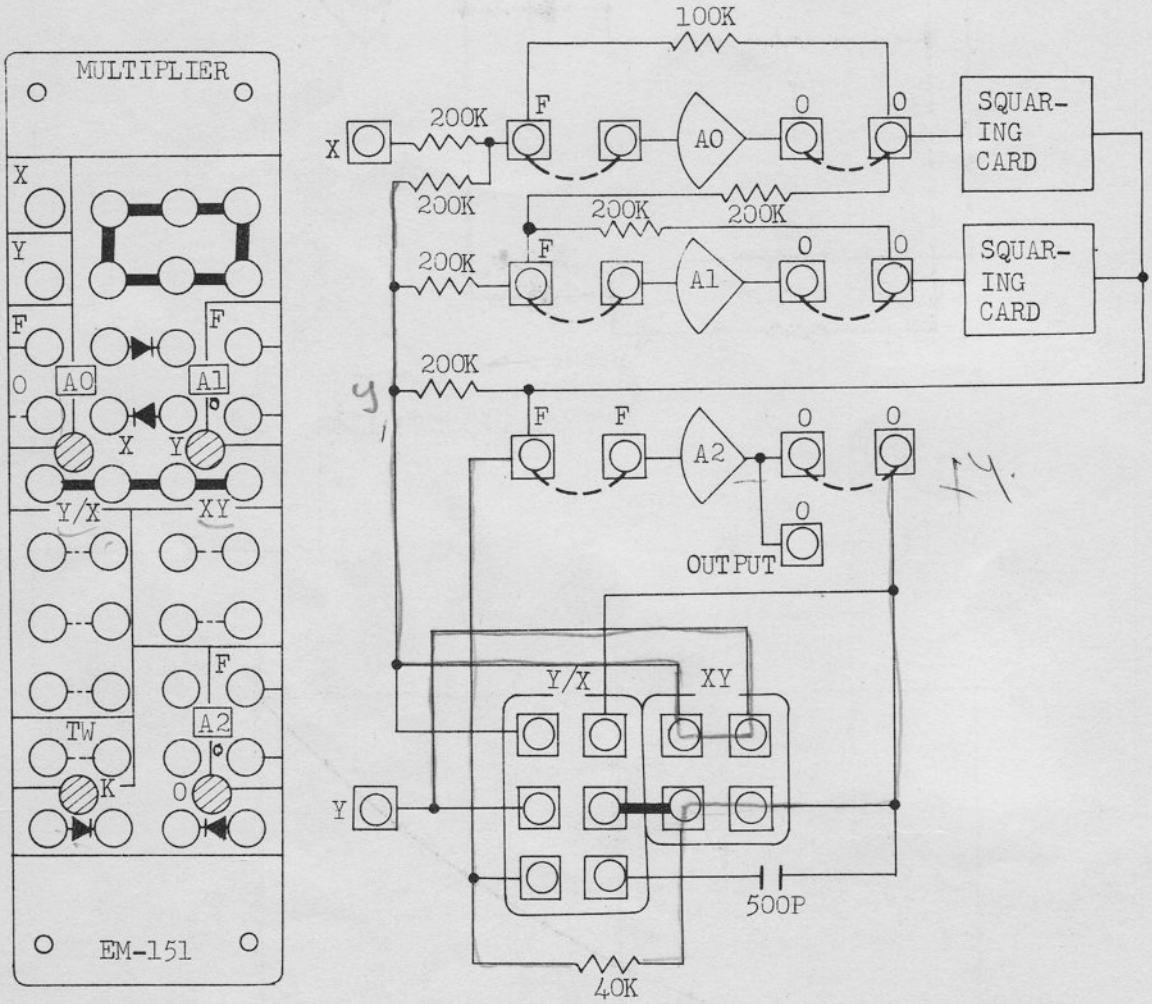
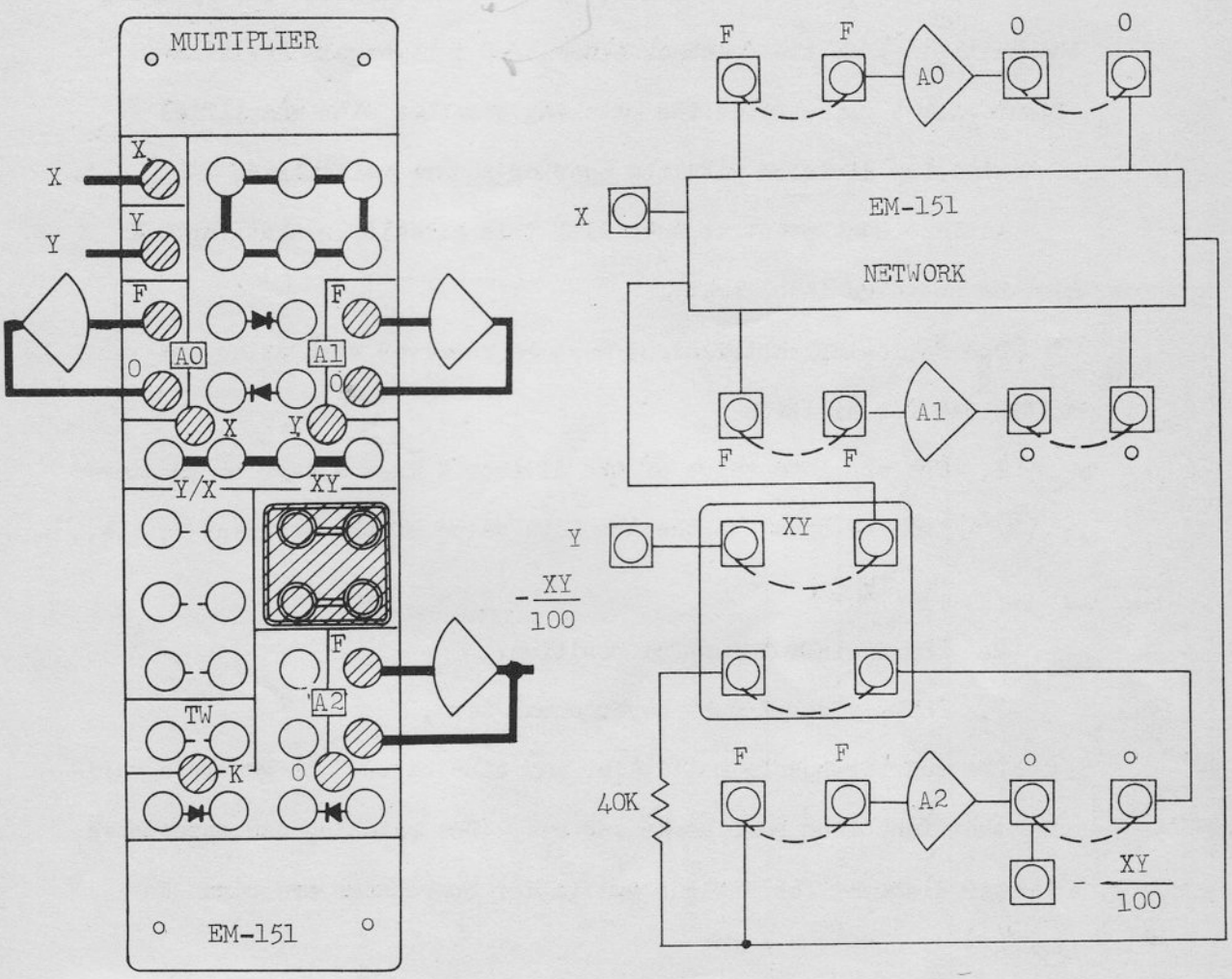


FIGURE 2.6-2 SQUARING CIRCUIT SIMPLIFIED SCHEMATIC



NOTE: AMPLIFIERS ARE NOT INCLUDED IN MULTIPLIER NETWORK EM-151

FIGURE 2.6-3 MULTIPLIER, SIMPLIFIED BLOCK DIAGRAM AND PATCHING BLOCK LAYOUT



TERMINALS "TW" SHOULD BE CONNECTED TOGETHER
IF DITHER SMOOTHING IS NECESSARY.

FIGURE 2.6-4 MULTIPLICATION PATCHING AND SIMPLIFIED SCHEMATIC

b. Division

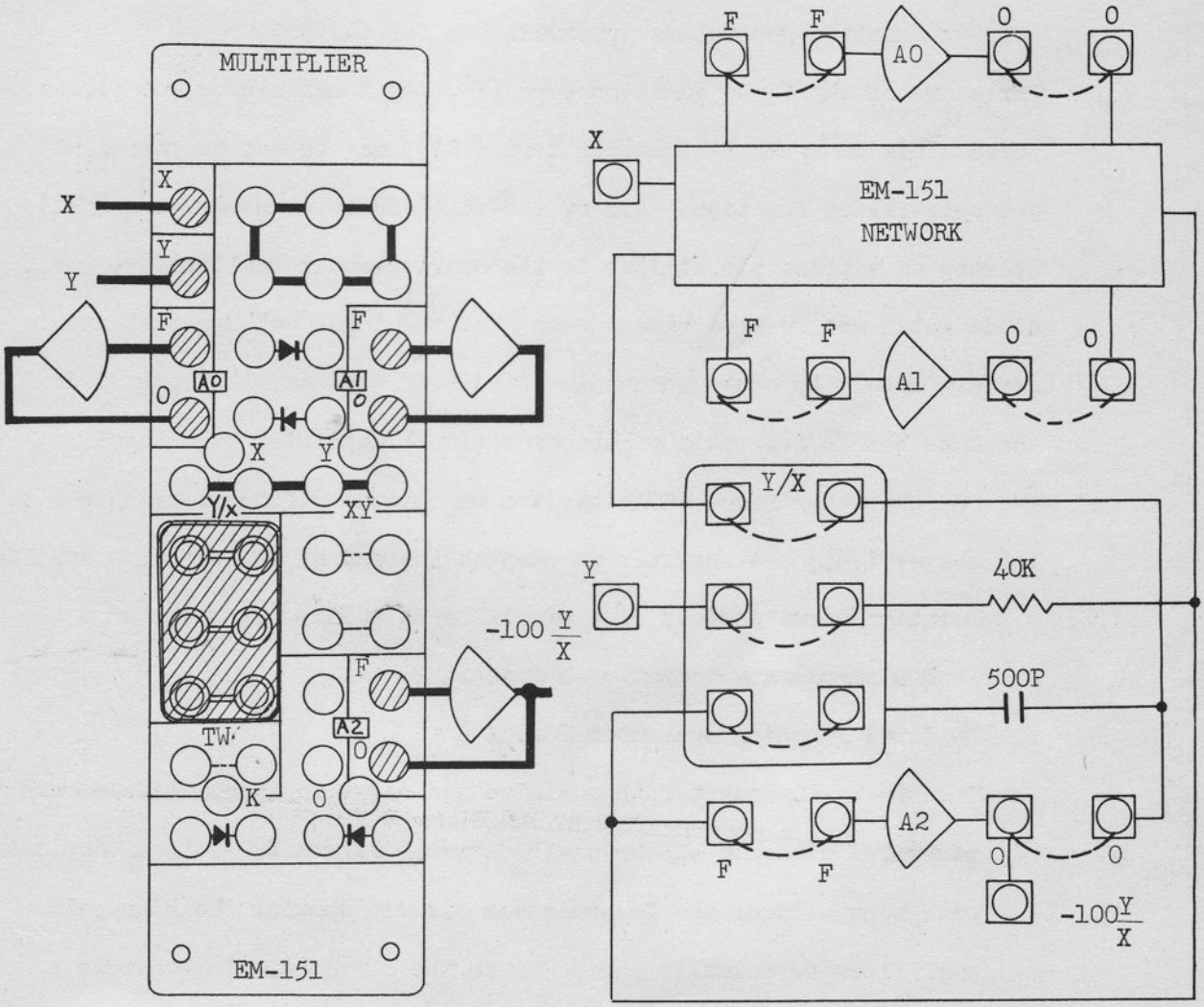
A variable (Y) may be divided by a second variable (X) by using the multiplier as the feedback element of a high-gain amplifier. Figure 2.6-5 illustrates the patching together with simplified schematic for division with the quarter-square multiplier.

An important point to note with this circuit is that input X must be positive in polarity.

The following restrictions must be observed when using the multiplier for division.

1. The absolute value of the divisor X must always be greater than or equal to the absolute value of the dividend Y; i.e., $|Y|/|X| \leq 1$.
2. The divisor X must be positive.
3. The divisor X must never equal zero.

The quarter-square multiplier may also be used to generate various other functions such as X^2 and etc. The patching and associated computer diagrams for various multiplier operations are given in Appendix 3.



NOTES: 1. X > Y
2. X > 0
3. X MUST BE POSITIVE

FIGURE 2.6-5 DIVISION PATCHING AND SIMPLIFIED SCHEMATIC

7. FUNCTION GENERATORS

Six function generators are available for the 505. Three are of the fixed function type (X^2, log X and sin or cos X), and three kinds of variable function type (VFG), may be set to represent a single-valued function. All of the fixed function generators (FFG) operate on a principle similar to the quarter-square multiplier; i.e., diode gates are reverse biased such that the input voltage must attain certain levels to cause succeeding diodes to conduct. As each diode conducts the Z_f/Z_{in} ratio of the operational amplifier is changed.

On the other hand, VFG's operate on quite a different principle to the above; i.e., a transistor is adopted instead of a diode, and supplies a suturation curve instead of a single break point. It gives an a operator a simple way to set up a function.

a. X^2 Fixed Function Generator FG-154 A

The 505 X^2 FG accept both positive and negative input voltages and generates either a $+X^2$ or a $-X^2$ output. Figure 2.7-1 is a simplified schematic of the X^2 generator circuit showing the high-gain amplifiers as normally patched into the circuits. To generate a $-X^2$ function a four-connector bottle plug must be placed as shown in Figure 2.7-2(b); i.e., the two upper terminations are connected to ether as are the two lower terminations. For $+X^2$ the connections should be made as shown in Figure 2.7-2(c).

Additional functions such as $\sqrt{X}$ are also obtainable with the X^2 FG. The patching and computer diagrams are given in Appendix 4.

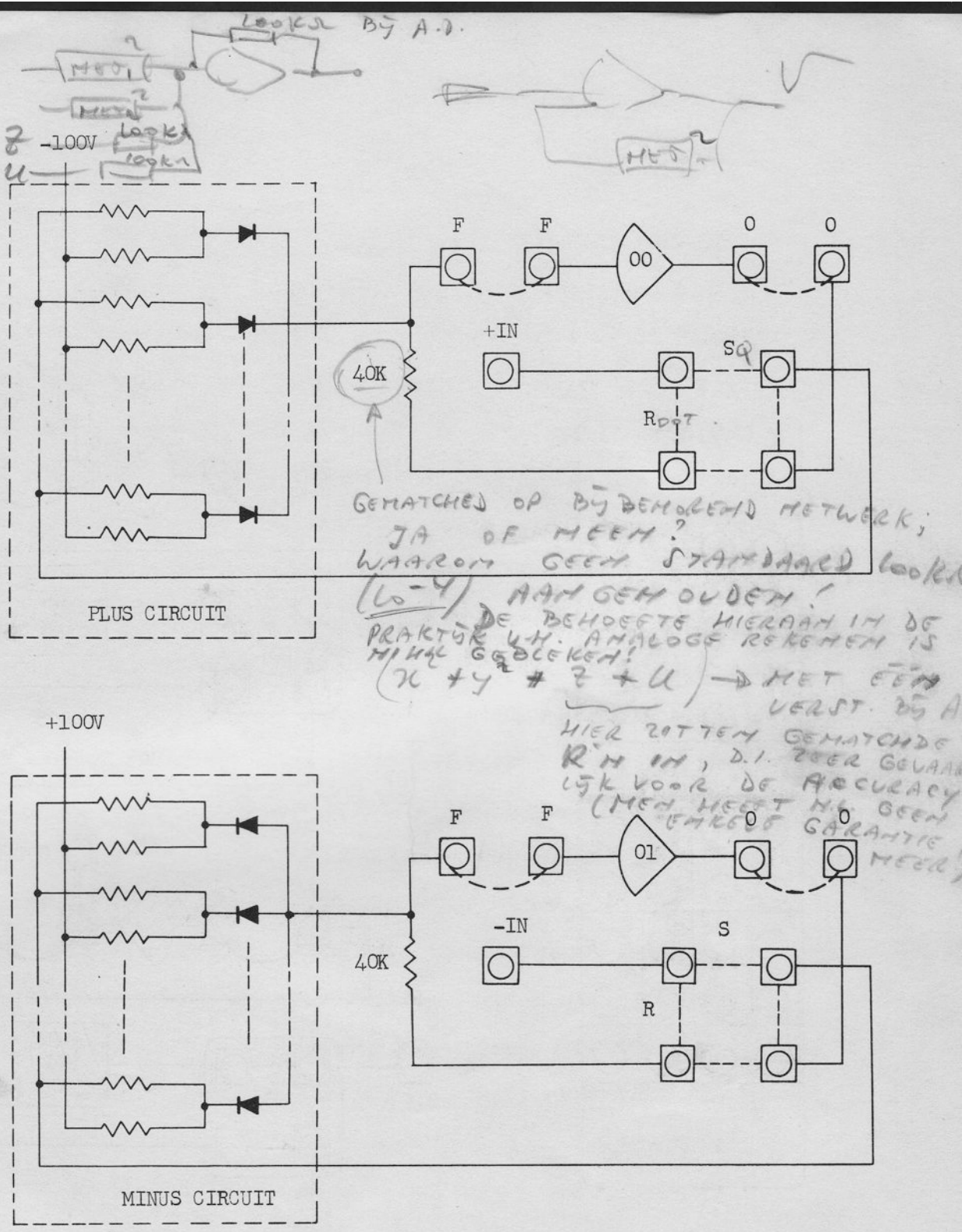
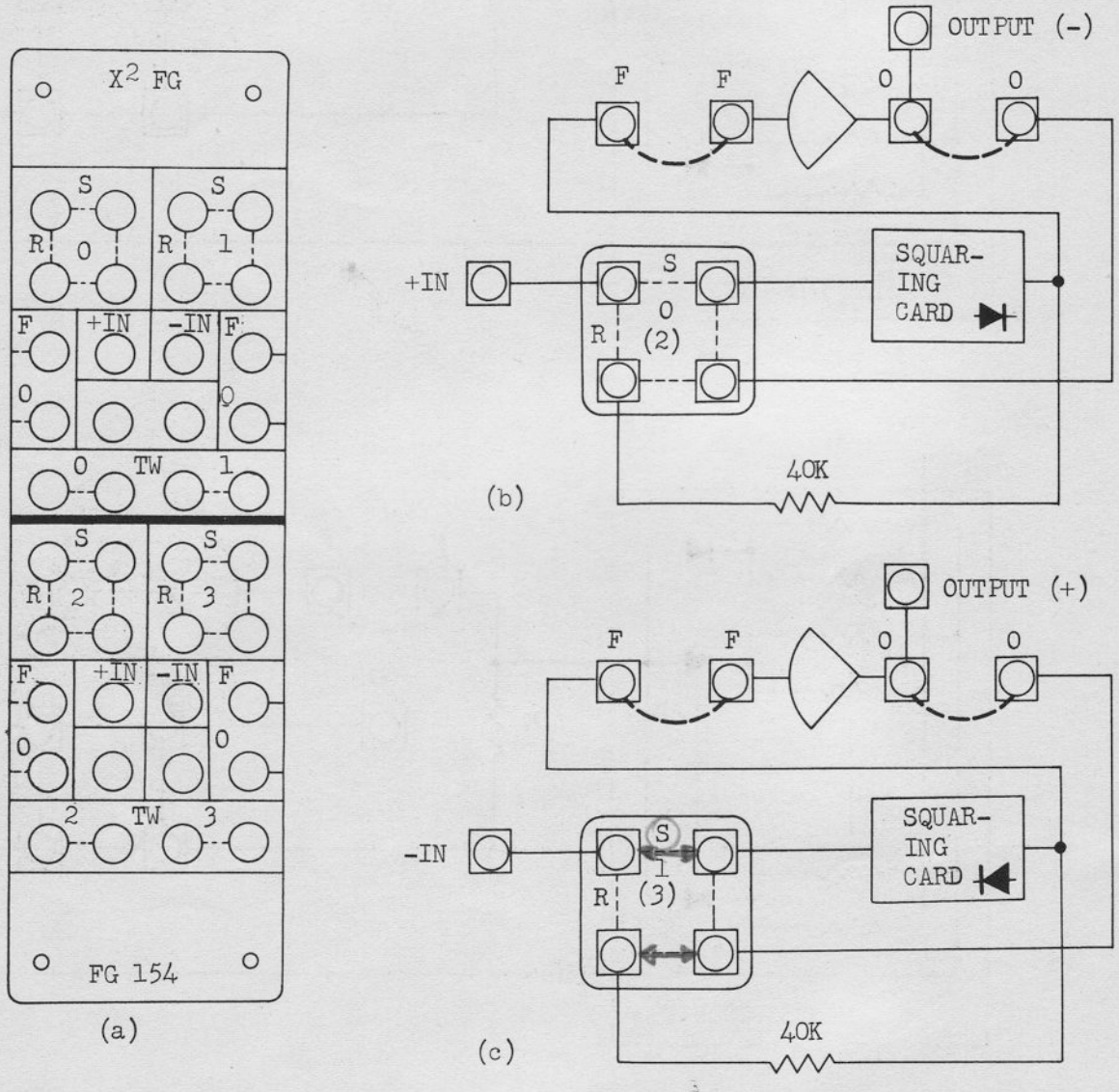


FIGURE 2.7-1 X^2 FG SIMPLIFIED SCHEMATIC



TERMINAL "TW" SHOULD BE CONNECTED TOGETHER IF DITHER SMOOTHING IS NECESSARY.

FIGURE 2.7-2 X^2 FG SIMPLIFIED SHCEMATIC AND PATCHING BLOCK

b. Log X fixed Function Generator FG-155A

The 505 Log X FG contains four individual log function generators all of which are terminated at the Pre-Patch Panel. Two of the generators accept only positive voltage input and two accept only negative voltage inputs. The output of the generators is the scaled logarithm to the base 1 (i.e., 50 log. |X|).

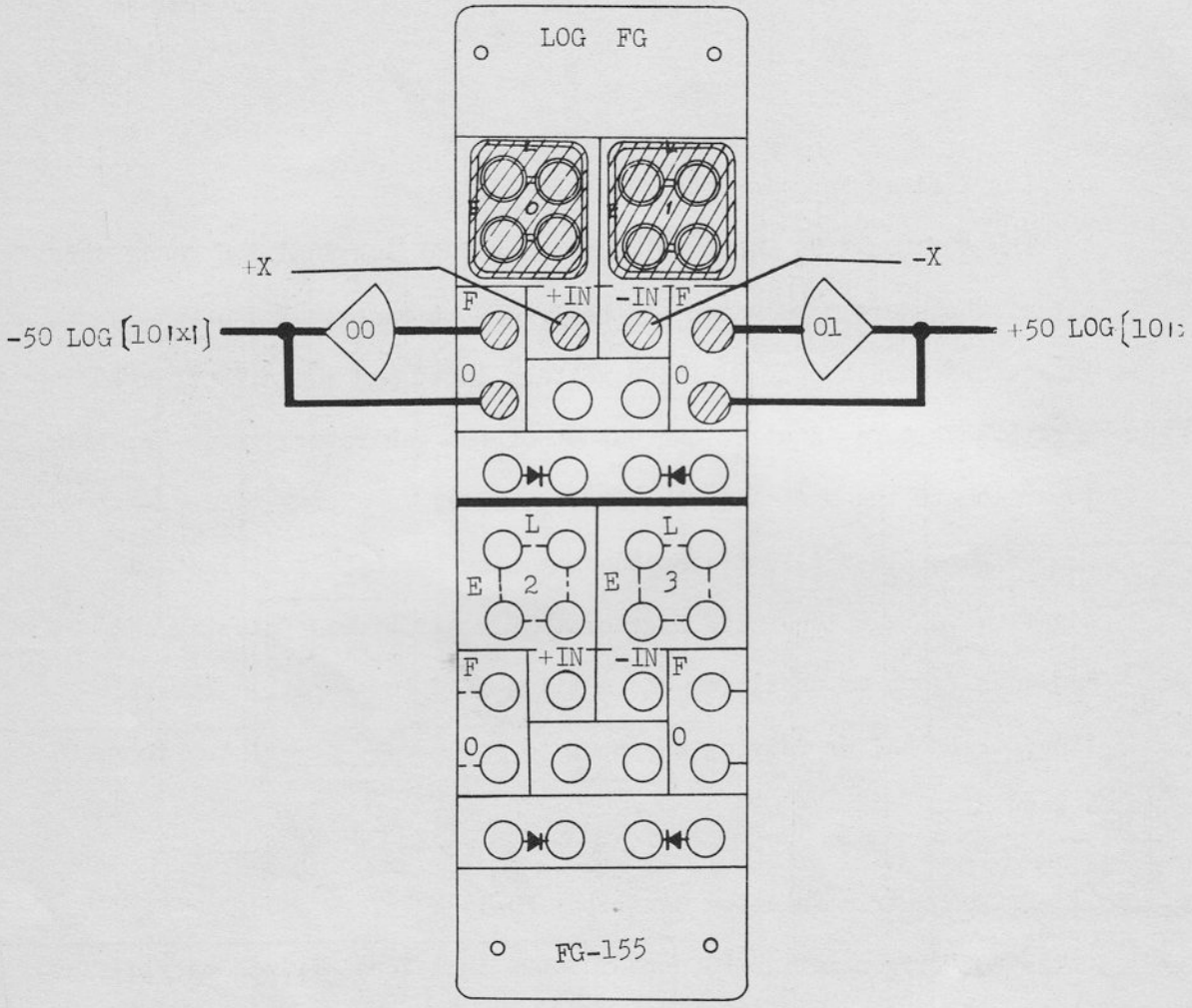
Figure 2.7-3 illustrates the patching for both positive and negative voltage input log X generators. Additional patching and FFG uses (such as obtaining the antilog of a log input, multiplication, division, or raising an input to an unusual power) are given in Appendix 5.

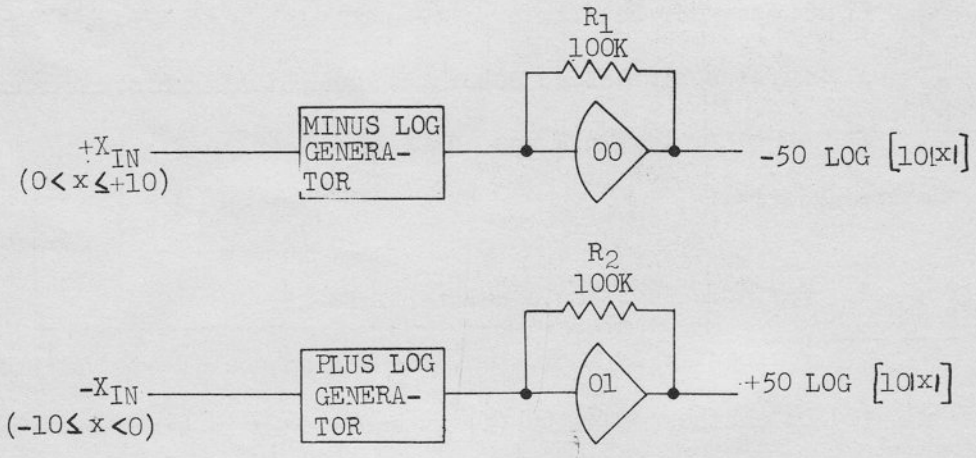
c. Trigonometric Function Generator FG-153A

The 505 Trigonometric FG contains two individual Trigonometric function generators both of which are terminated at the Pre-Patch Panel. Each generator accepts a voltage of eather polarity. Figure 2.7-4 illustrates simplified schematic and patching block layout. Patching to generate sin X and cos X are given in Figure 2.7-5 and 2.7-6 respectively.

d. Variable Function Generator FG-151

Frequently in a problem, the dependence of one variable quantity (Y) on another quantity (X) is known only in the form of experimentally obtained data. The Variable Function Generator (VFG) provides a means, with a single component of approximating and generating functions of this type.

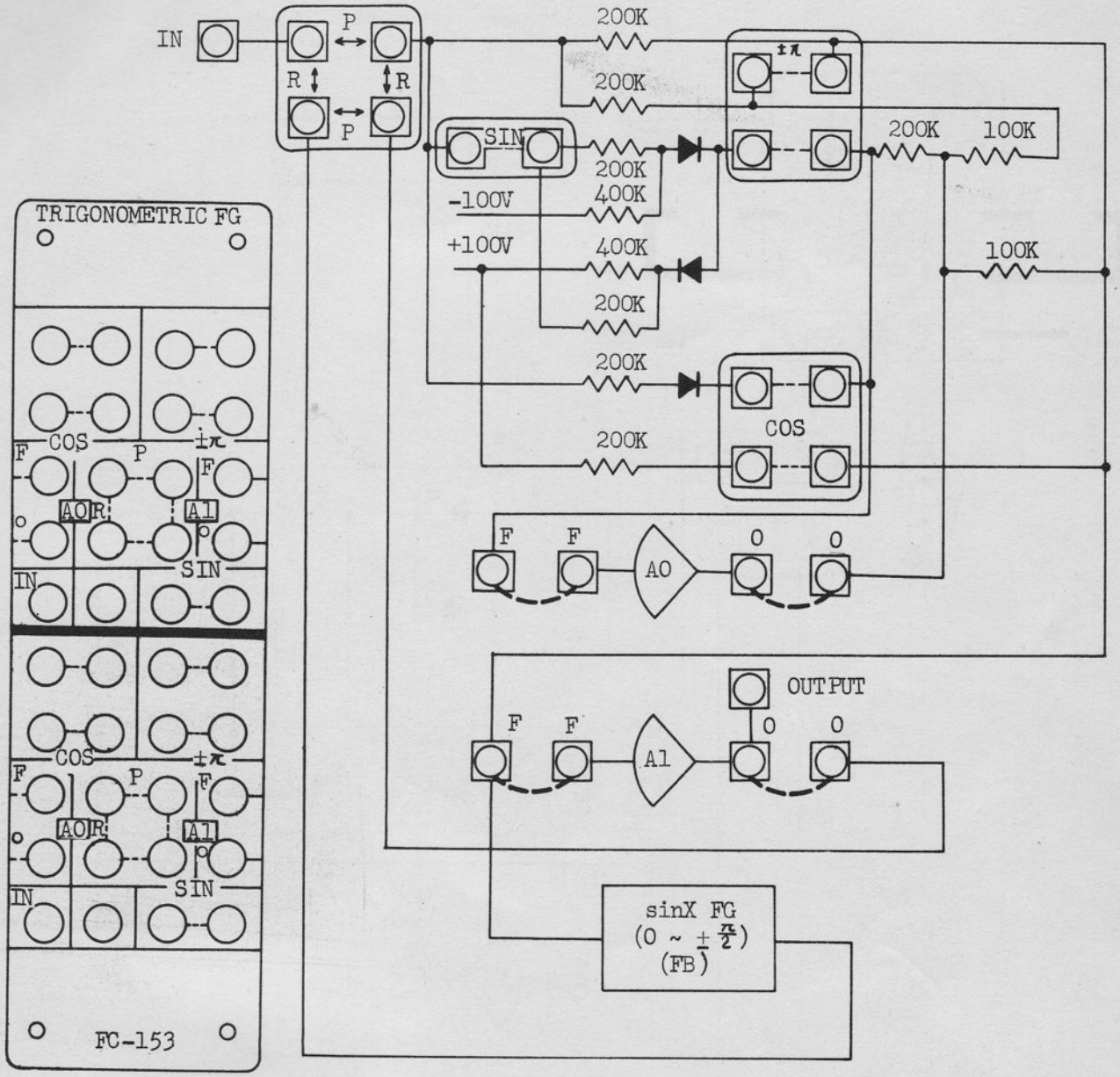




NOTE:

1. R_1 AND R_2 OHMS IN ALL CASES.
2. OUTPUTS ARE LOG TO BASE 10.

FIGURE 2.7-3 LOG X FG PATCHING AND SIMPLIFIED SCHEMATIC



NOTE: THE SIMPLIFIED SCHEMATIC CORRESPONDS HALF OF THE PATCHING FG-153

FIGURE 2.7-4 TRIGONOMETRIC FG, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK LAYOUT

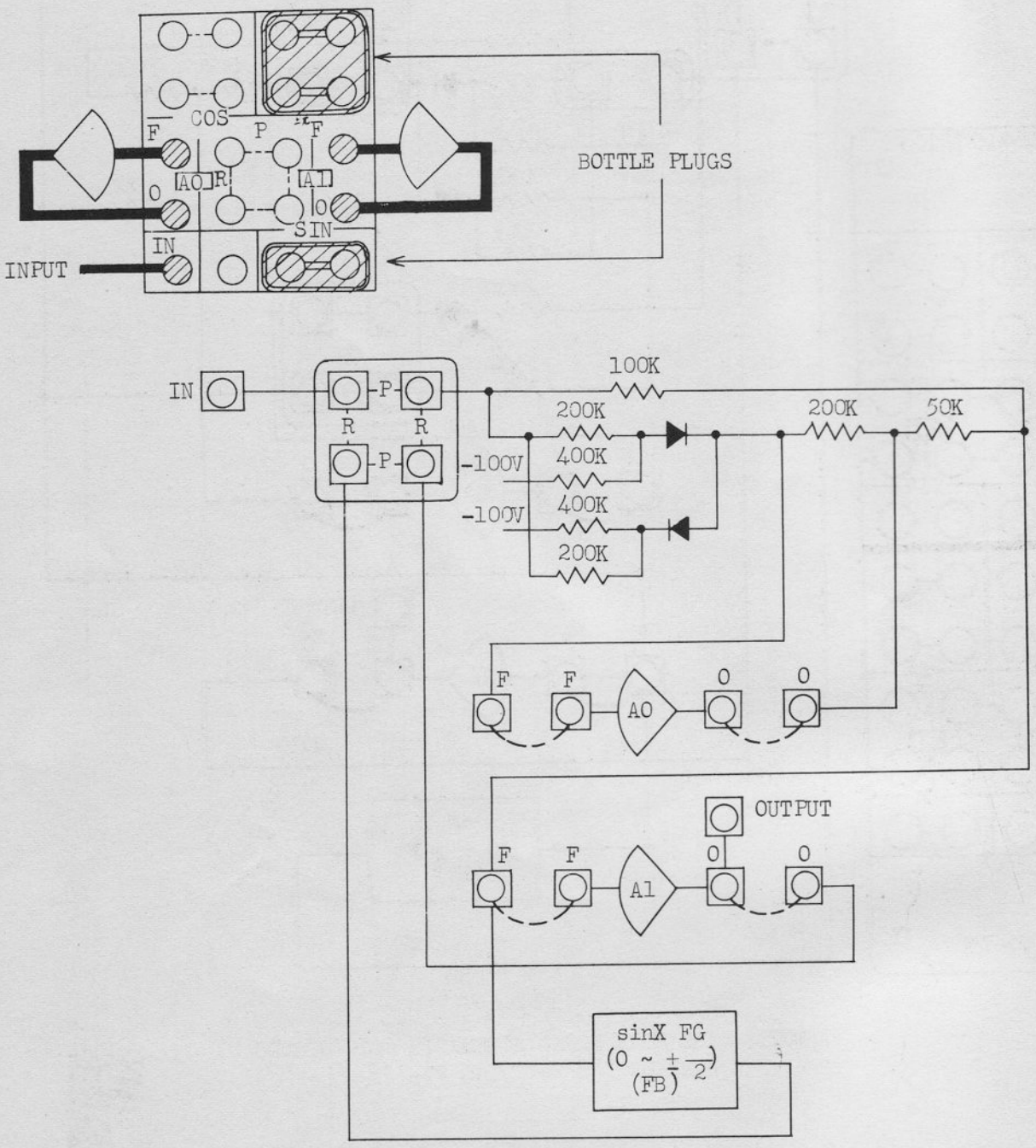


FIGURE 2.7-5 sinX PATCHING AND SIMPLIFIED SCHEMATIC

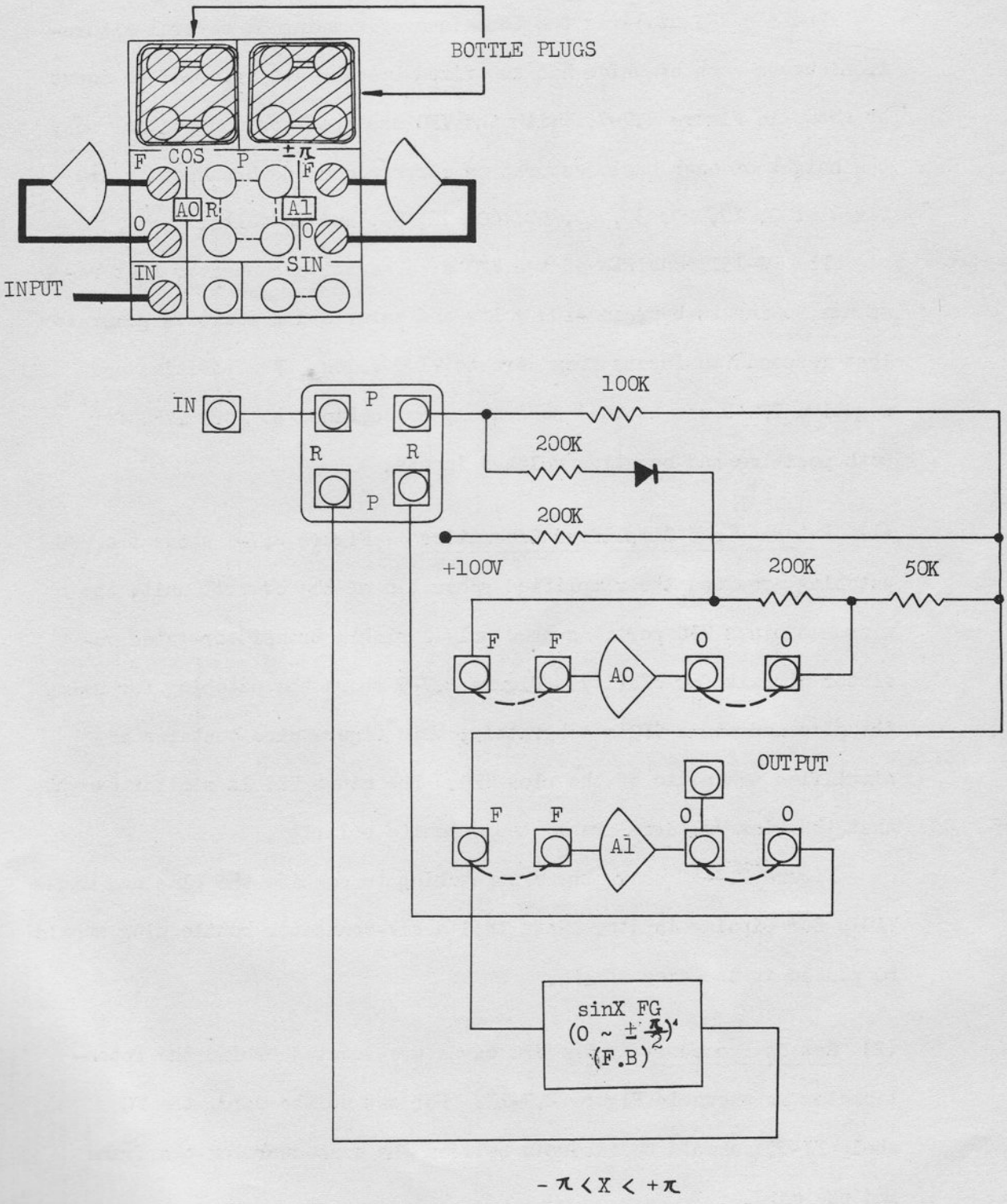


FIGURE 2.7-6 cosX PATCHING AND SIMPLIFIED SCHEMATIC

The 505 VFG utilizes the technique of summing of several saturation curves each of which has two fixed breakpoints referred to input as shown in Figure 2.7-7. With the VFG the operator can control only the height of each basic saturation curve since the breakpoints are fixed at 0, 10, 20, 30, 40, 50, 60, 70, 80, and 90 volts.

The FG-151 consists of two VFG's: a negative generator that responds to inputs between -100 volts and zero, and a positive generator that responds to inputs from zero to +100 volts. The positive and negative VFG's can be used separately or combined to form ±VFG for both positive and negative voltage inputs.

(1) Patching and Simplified Schematics Figure 2.7-8 shows the VFG patching area and the simplified schematic of the overall unit; the plus and minus VFG portions show only a single transistor-gated resistor circuit for clarity. Figure 2.7-9 shows the patching for using the plus and minus VFG's separately; this figure also contains a simplified schematic of the plus VFG. The minus VFG is similar except that the bias voltages are in the opposite polarity.

Figure 2.7-10 shows the VFG patching to combine the plus and minus VFG's for bipolar inputs. Note that a six-connector bottle plug should be placed in the area of ±FG.

(2) Set Up Procedure The VFG cards are located behind the Potentiometer as shown in Figure 2.7-11. For set up the card, the FG shelf FJ-051 should be inserted between the connectors on the frame and the card.

Each VFG unit has eleven adjustments; They are all F(X) potentiometers to adjust the output of curve height between unitary, incremental inputs of X.

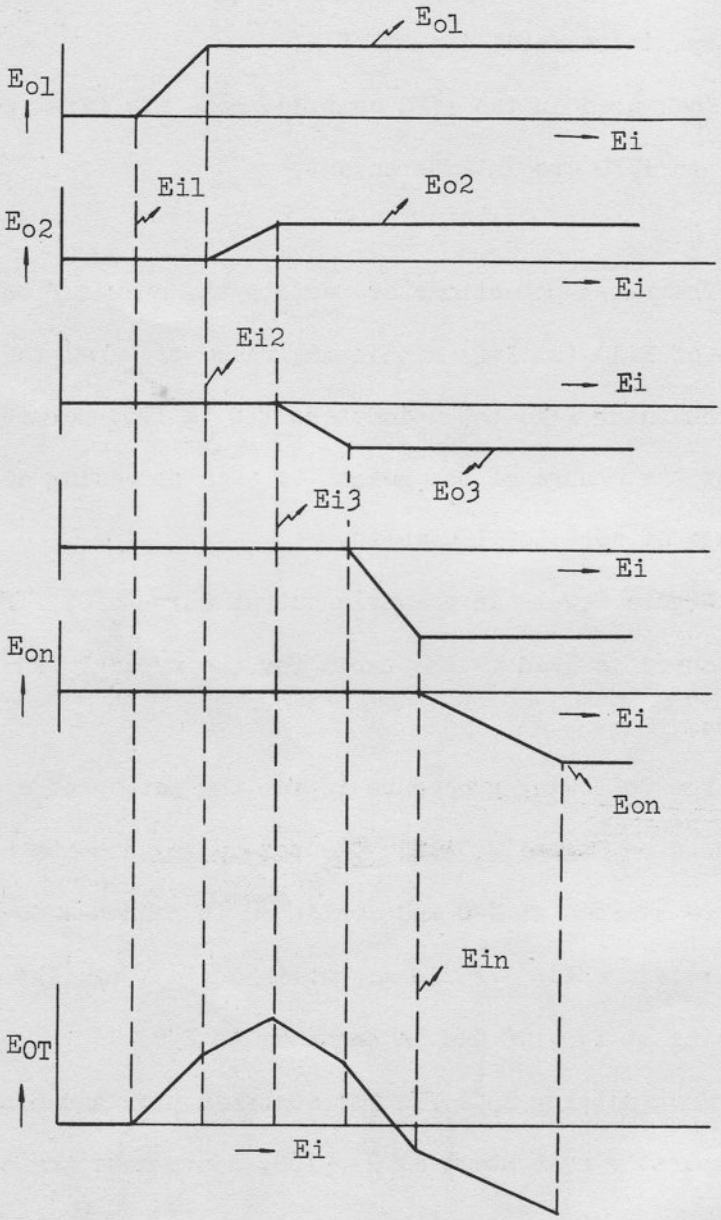
When used in the ±VFG combined mode the first pots of the -VFG and +VFG are interdependent.

The first potentiometer permits the operator to set the value of F(X) (at X=0) within the range of +100 to -100 volts. The remaining F(X) potentiometers (10 to 100) permit the operator to set the change of the height to each preceding segment by a voltage of zero to ±100 volts.

Figure 2.7-12 is a sample output curve of a +VFG. This curve is used as the basis for the typical VFG set-up procedure.

The following procedure is for the set-up of a +VFG patched as shown on Figure 2.7-12. The set-up adjustments of the +VFG must be started at X=0 and continued in sequence to X= +100. The procedure for -VFG is accomplished in a similar manner, but starting at X= -100 and in sequence to X=0.

When setting up a VFG for combined plus and minus inputs the operator must start at X= -100, don't make the set-up of X=0 in plus VFG.



$$E_{OT} = \sum_{n=1}^{N} E_{on}$$

FIGURE 2.7-7 PRINCIPLE OF VFG

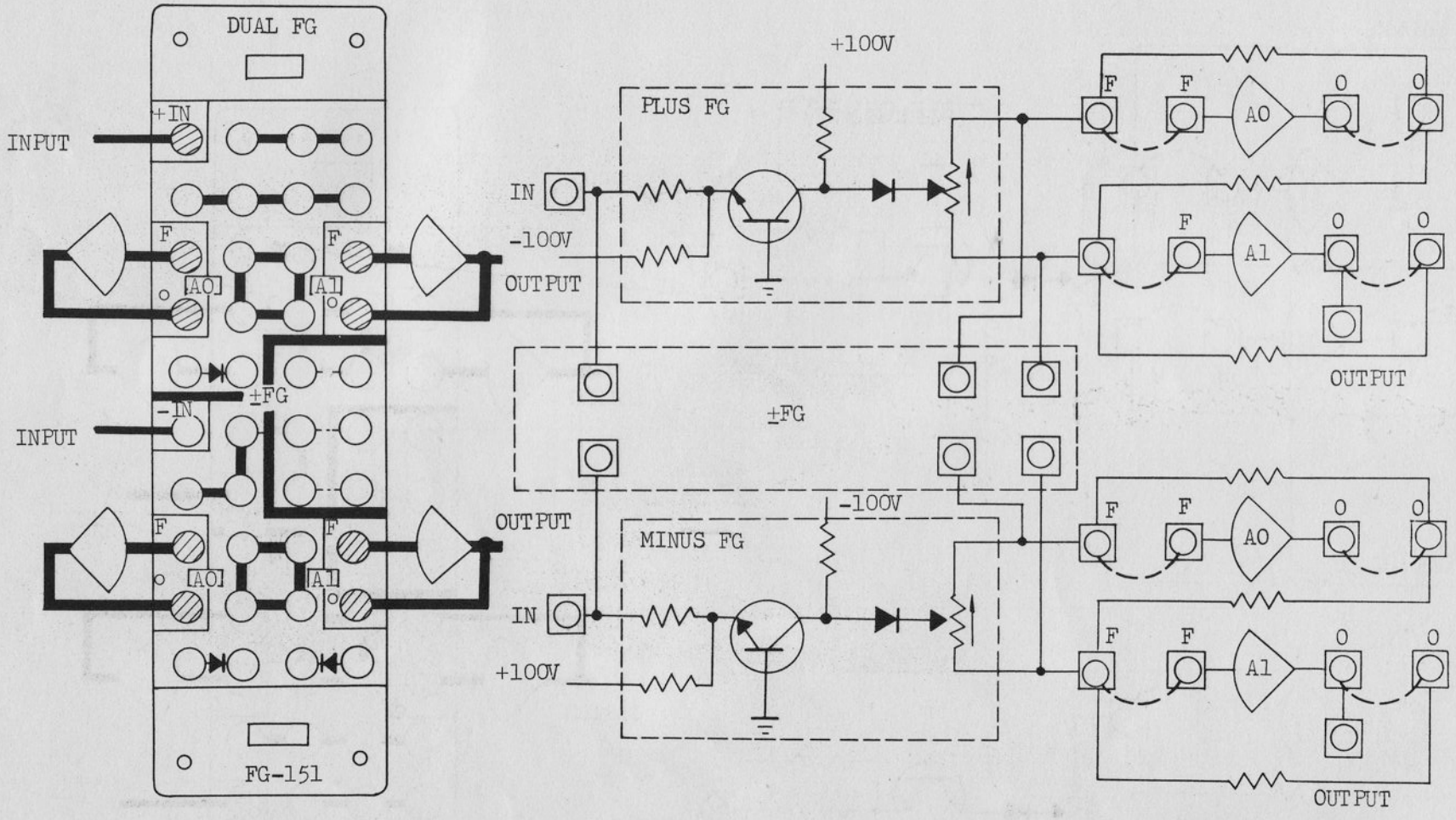


FIGURE 2.7-8 VFG FG-151, SIMPLIFIED BLOCK DIAGRAM AND PATCHING BLOCK

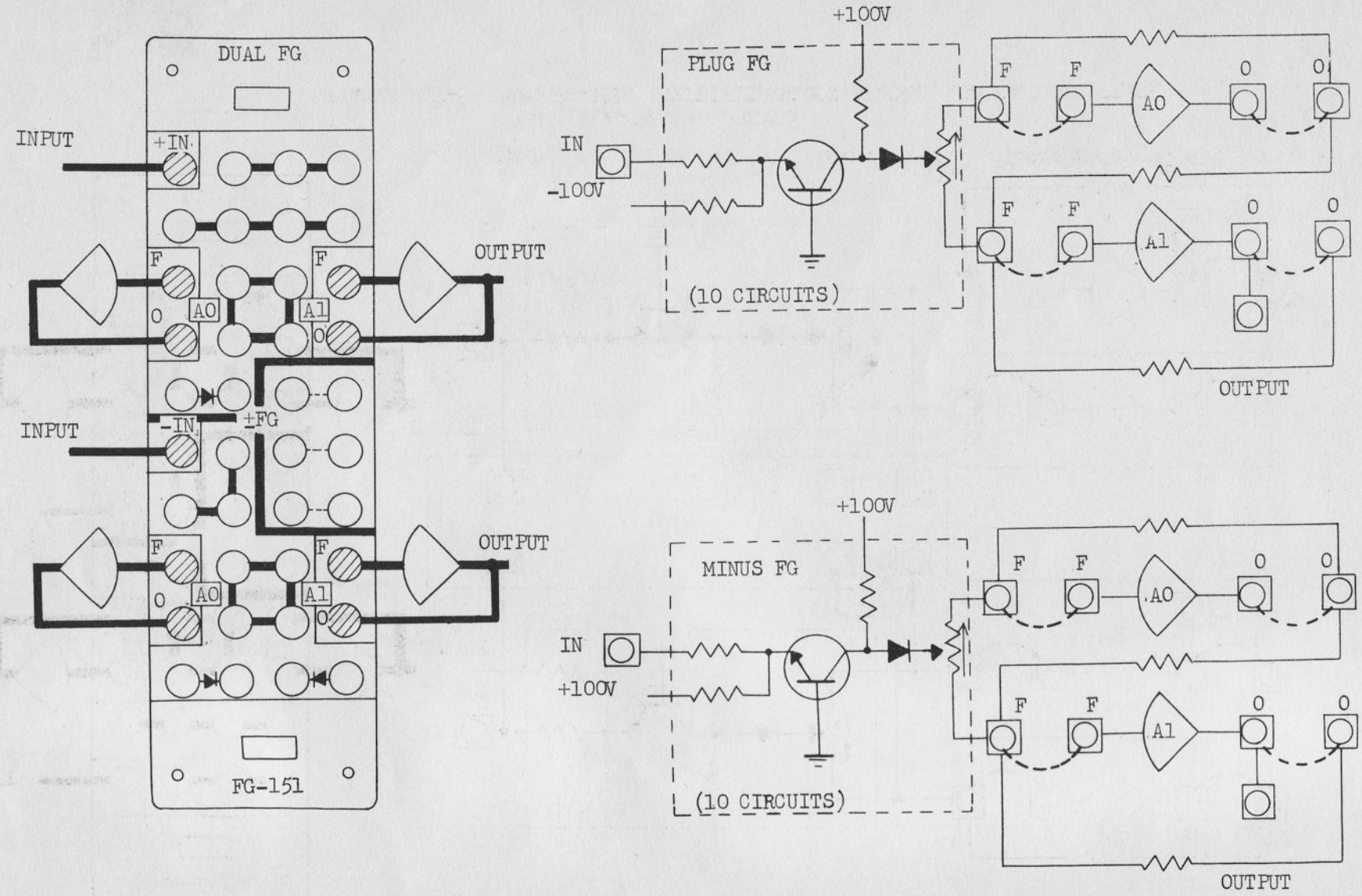
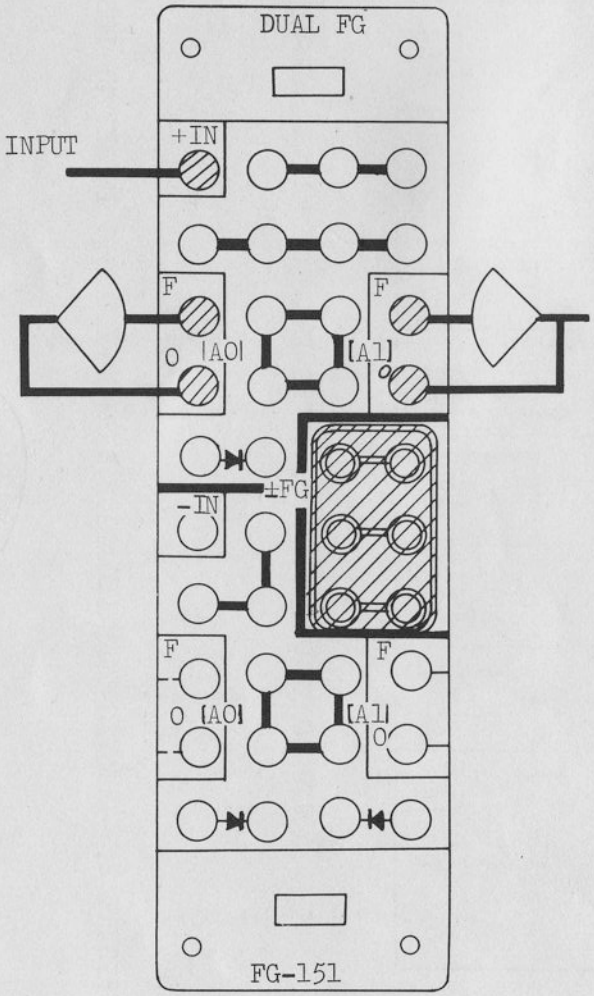
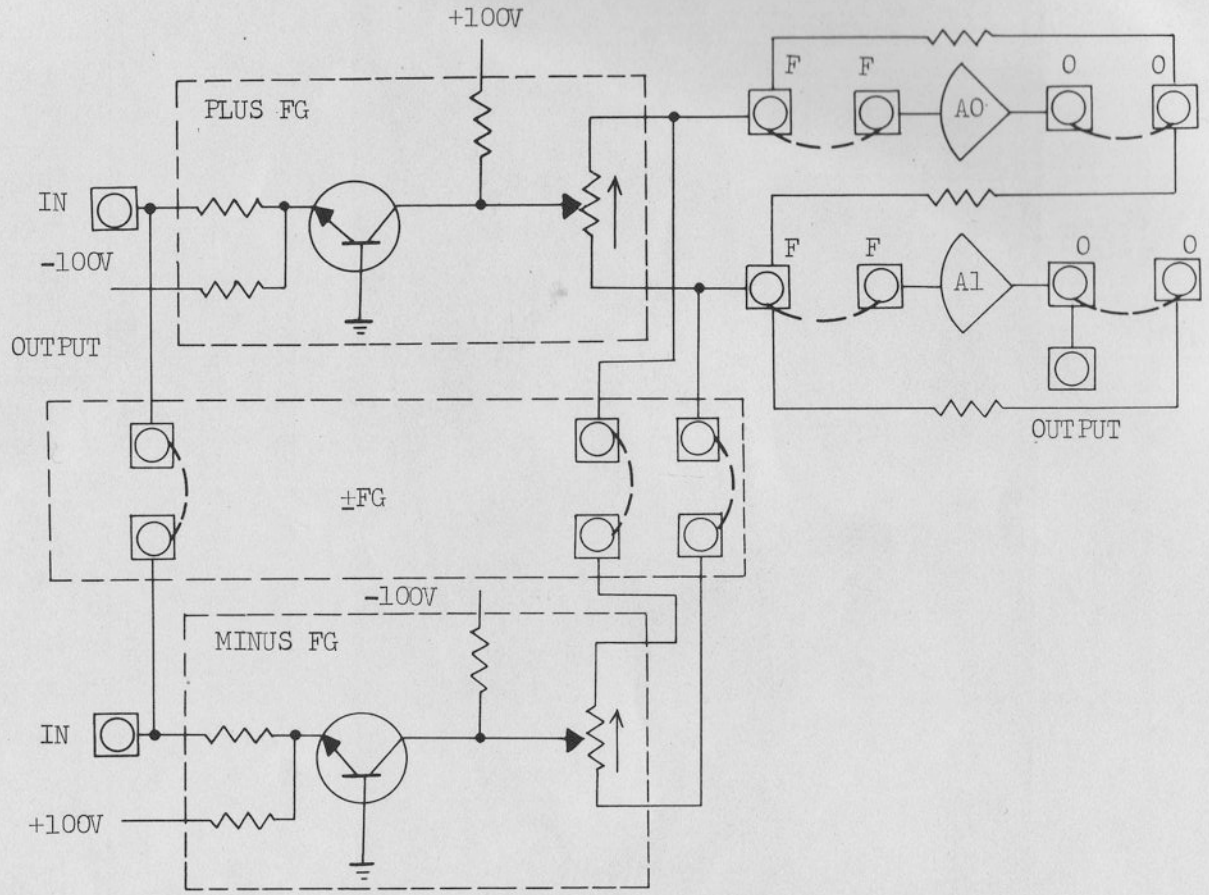
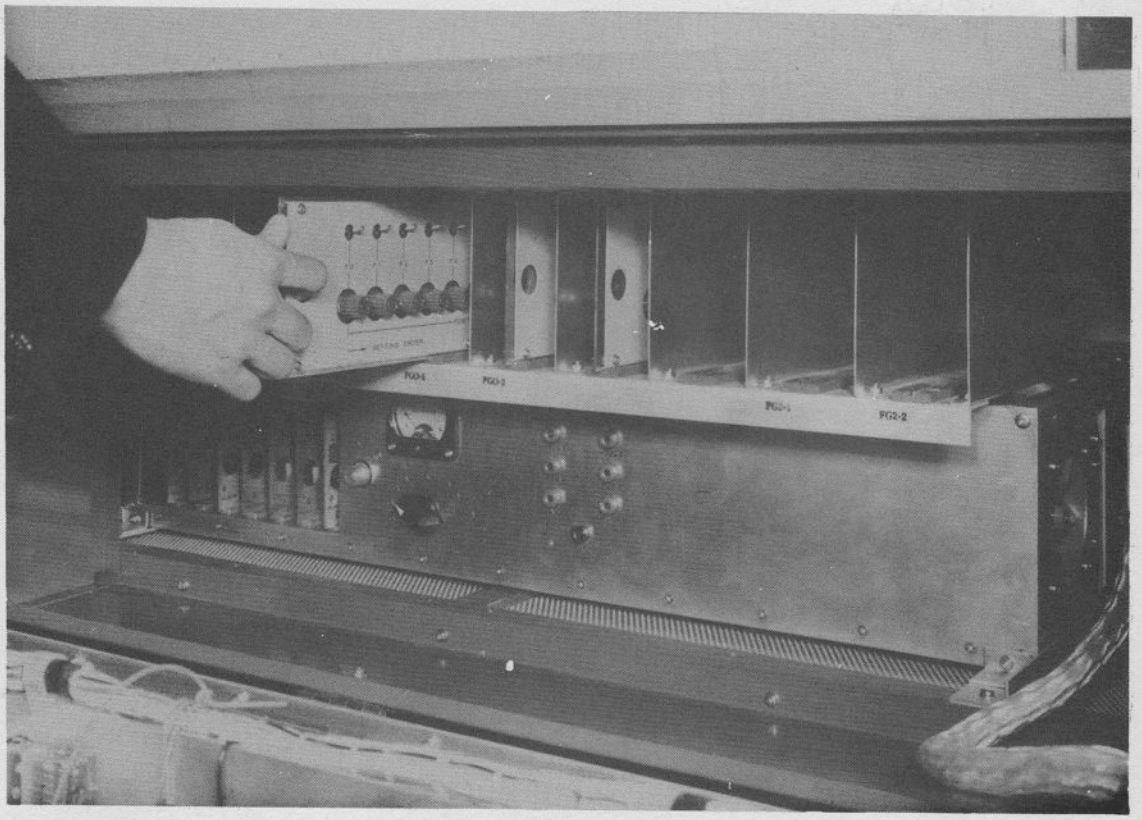


FIGURE 2.7-9 VFG FG-151, SEPARATE VFG PATCHING





SLECHTS 2 AMP'S ALS ± KAARTEN WORDEN GECOMBINEERD.



a. VFG CARD LOCATION

PRE-PATCH PANEL AREAS		VFG LOCATIONS						
		FG03	FG0-1	FG0-2	FG1-1	FG1-2	FG2-1	FG2-2
OVER-LOAD AMPL	DITH-ER		FG-051A	FG-051B	FG-051A	FG-051B	FG-051A	FG-051B
			OR	OR	OR	OR	OR	OR
OI-051	TW-051	FG-057	FG-052	FG-052	FG-052	FG-052	FG-052	FG-052

b. VFG LOCATIONS AND ASSOCIATED PRE-PATCH PANEL AREAS

FIGURE 2.7-11 VFG CARD LOCATION SHOWING CHASSIS IN SET UP POSITION

(3) Typical VFG Set-Up Procedure

(a) Insert the FG shelf between the connectors on the frame and the card.

(b) Select the F(X) amplifier output (designated A1 on Figure 2.9-9) for readout on the DVM (or multi-range voltmeter if the DVM is not available).

(c) Turn the "SET-OPE" switch on the card to "SET" side, and turn all "SET-RESET" switches to "RESET" side.

(d) Turn the "SET-RESET" switch of F0 to "SET" side and adjust the F0 potentiometer by matching the output to the value of F(0).

(e) Turn the "SET-RESET" switch of F1 to "SET" side and adjust the F1 potentiometer by matching the output to the value of F(1).

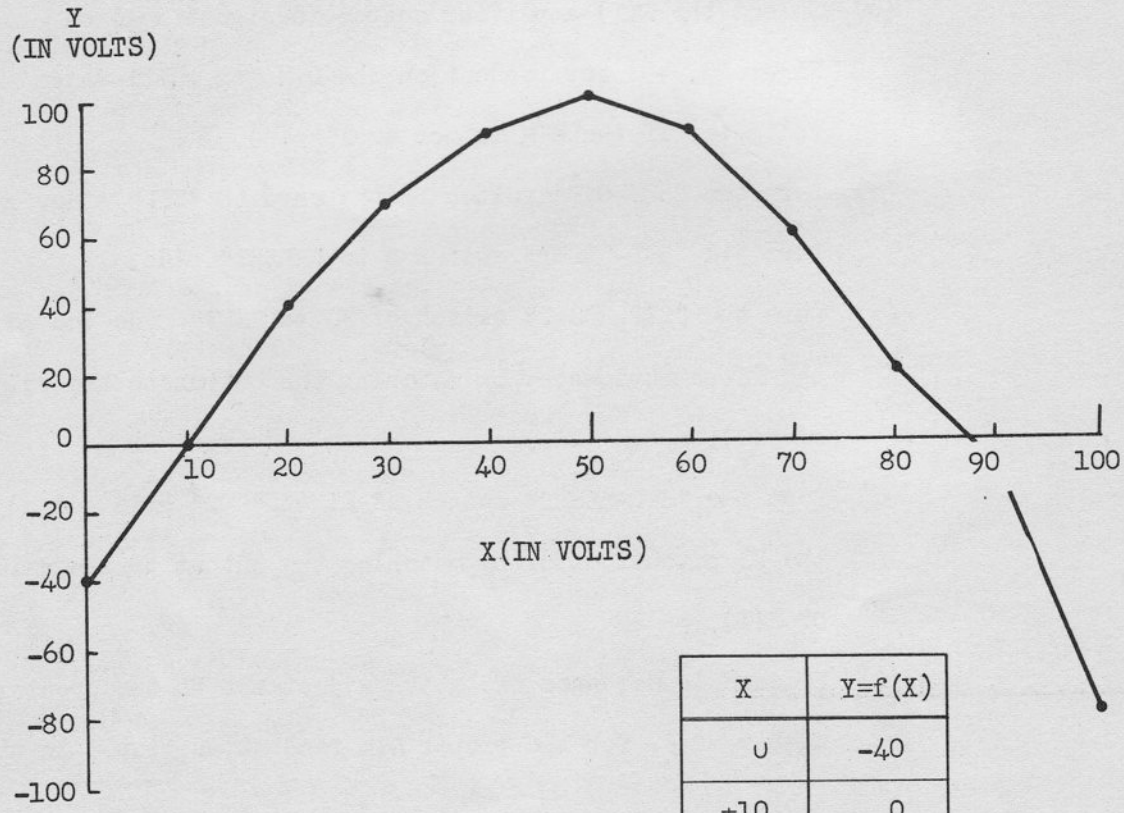
(f) Proceed in sequence the above adjustment to the greater number of F, for the proper DVM readout as listed in the table.

(g) For optimum accuracy repeat the set-up procedure, starting with step (c).

(h) Turn the "SET-OPE" switch on the card to "OPE" side.

e. Variable Function Generator FG-152

The VFG FG-152 is the same to the VFG FG-151 except the breakpoints. The breakpoints of the FG-152 are -100, -80, -60, -40, -20, 0, 20, 40, 60, 80 and 100 volts. Therefore, the FG-152 covers by itself the whole input range.



X	Y=f(X)
0	-40
+10	0
+20	+40
+30	+70
+40	+90
+50	+100
+60	+90
+70	+60
+80	+20
+90	-10
+100	-80

FIGURE 2.7-12 SAMPLE VFG OUTPUT CURVE

The function card of the FG-152 is called FG-052, and two FG-052 cards are terminated on the FG-152 patching area.

f. Variable Function Generator FG-157

The Variable Function Generator FG-157 is a versatile device which makes it possible to set up the both coordinates Xn and F(Xn) of each set point n independently. Therefore, with the FG-157, the operator can control both the breakpoint and the height of a given function quite easily. Moreover, each adjustment can be done independently even in same kind of coordinate, so it is very easy to change a portion of the set-up function.

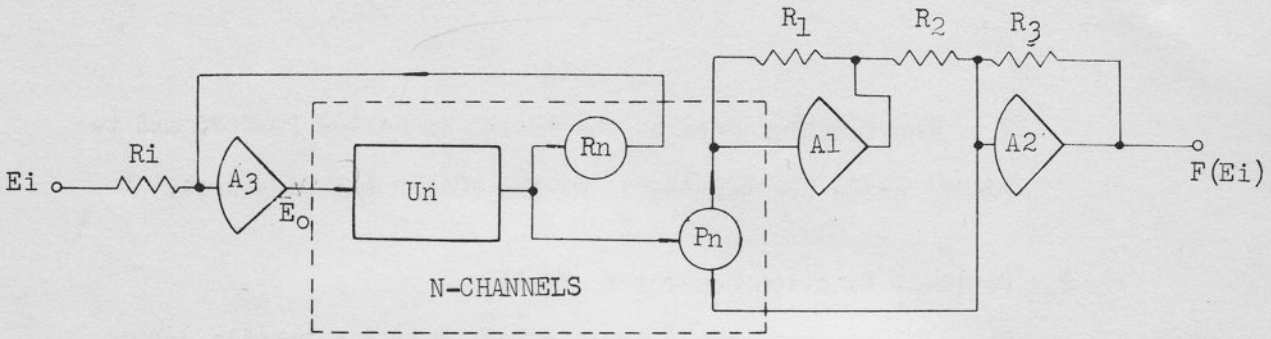
The principle of the FG-157 is explained on Figure 2.7-13. Figure 2.7-14 illustrates the patching for ordinary use of the Function generator.

The following procedure is for the set-up of a FG-157 for positive input patched as shown on Figure 2.7-12. The set-up adjustments of the FG-157 must be started at F0 and continued in sequence to F10 on the function card FG-057.

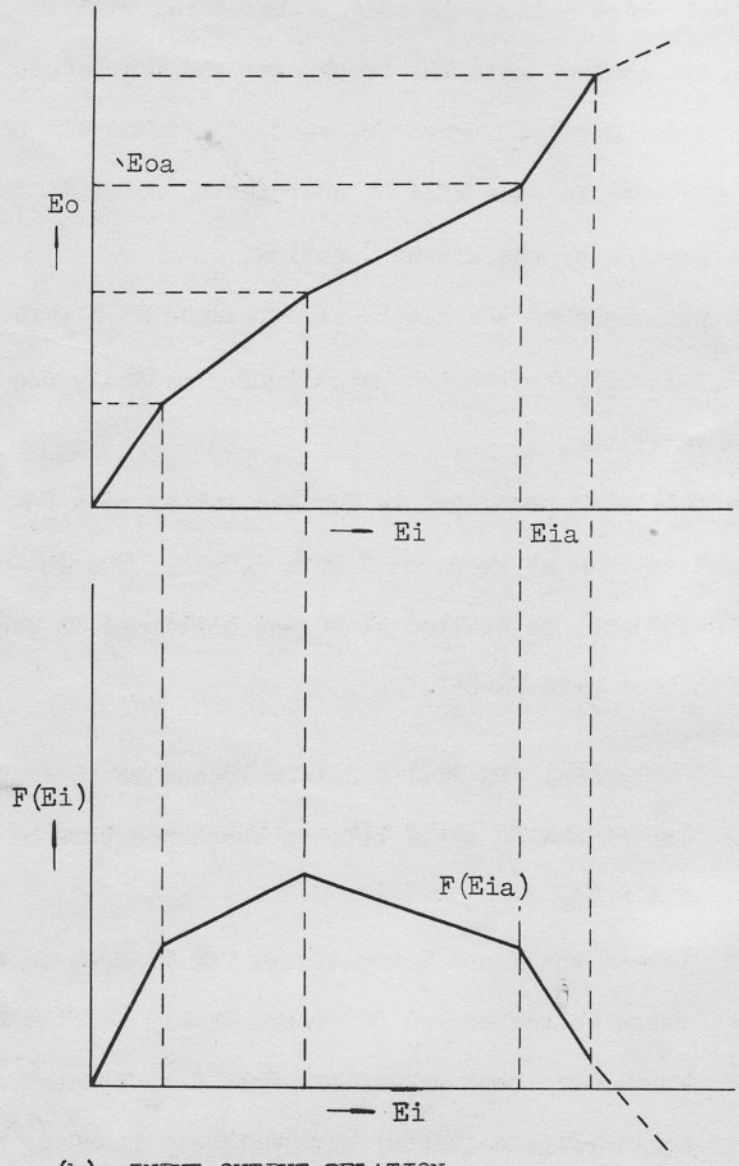
Typical VFG FG-157 Set-Up Procedure

(a) Insert the FG shelf between the connectors on the frame and the card.

(b) Select the X and Y amplifiers for readout on the multi-range voltmeter and DVM respectively (if the DVM is not available, both amplifiers should be connected to the multi-range voltmeter alternatively by using the selector system or the function switch.



(a) SIMPLIFIED BLOCK DIAGRAM



(b) INPUT-OUTPUT RELATION

FIGURE 2.7-13 PRINCIPLE OF VFG FG-157

(c) Turn "OPE-SET" switch to "SET" side and all "SET-RESET" switch to "RESET" side. Keep "+INPUT — ± INPUT" switch to "+INPUT" side.

(d) Put up the F0 switch to "SET" side and adjust the value of Y and X potentiometers by matching both outputs to the valve of Y1, Xo. Put down the F0 switch to "RESET" side after the adjustments mentioned above.

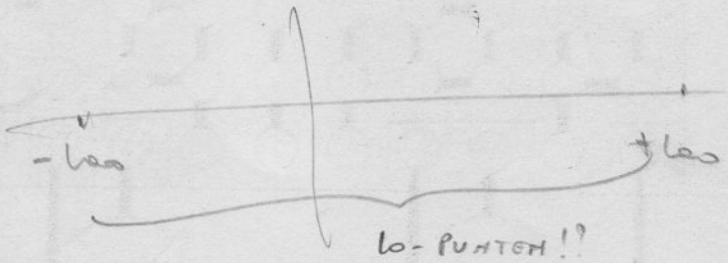
(e) Put up the F1 switch to "SET" side and adjust the value of Y and X potentiometers by matching both outputs to the value of Y_1, X_1. Put down the F1 switch to "RESET" side after the adjustments mentioned above.

(f) Proceed in sequence the above adjustment to the greater number of F, for the proper voltmeter and DVM readings as listed in the table. Note that the value of Xn should not exceed the value of X_{n+1} in the above settings.

(g) Turn "OPE-SET" switch on the cord to "OPE" side.

If the both polarity of input is necessary, set up the function by the procedure mentioned above, and after that, expand the input range by turning "+INPUT — ±INPUT" switch to "+INPUT" side.

It is recommended that the FG-057 should be used for positive input, if the function is defined for a single input polarity.



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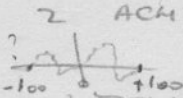

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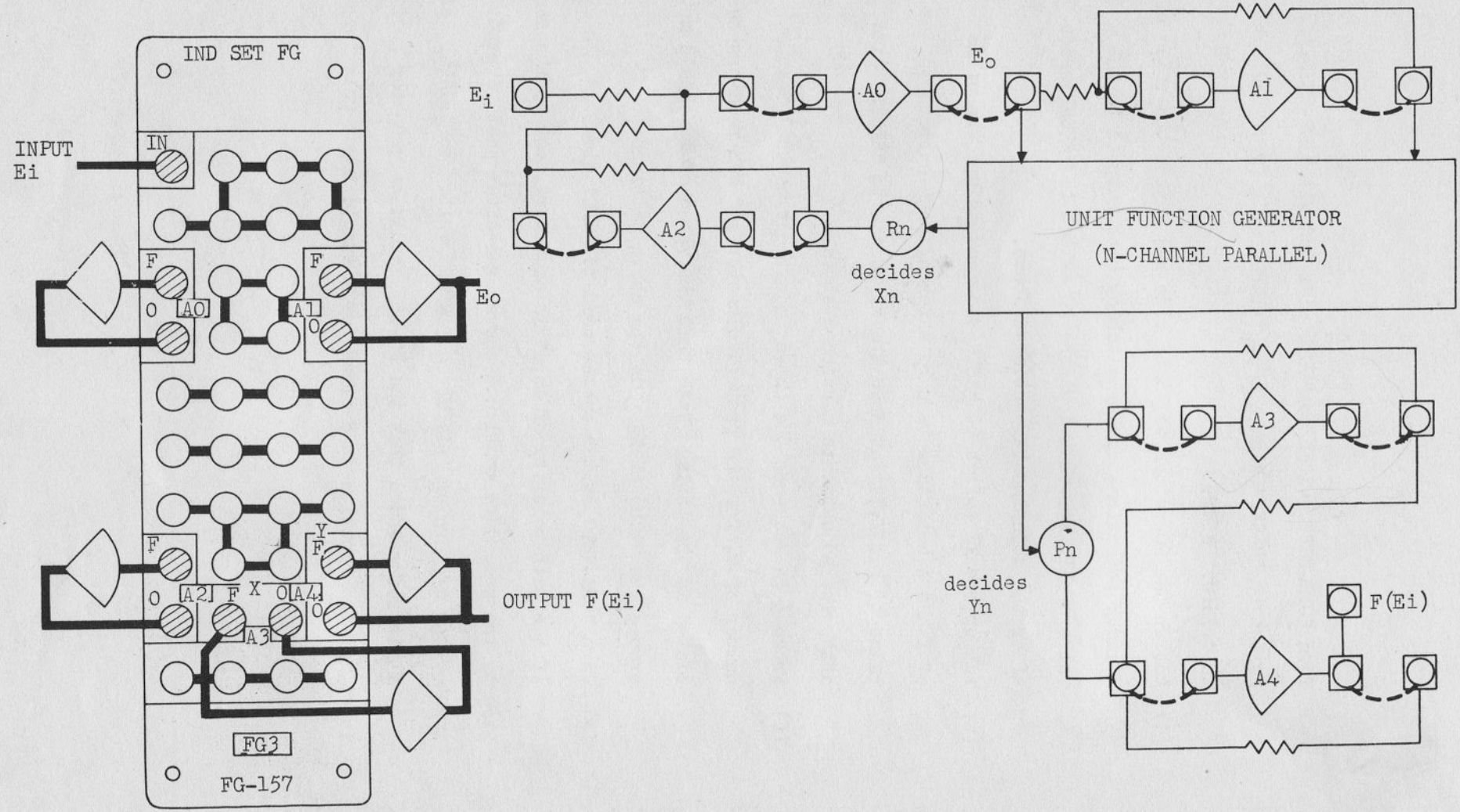


FIGURE 2.7-14 FG 157, SIMPLIFIED BLOCK DIAGRAM AND PATCHING BLOCK

8. COMPARATORS CP-151, CP-152

The signal comparator is an automatic switching device that consists of a comparator amplifier and a double-pole, double-throw relay. The amplifier compares two input voltages and energizes or de-energizes the relay, depending on whether the sum of the input voltages is greater than zero (positive) or less than zero (negative).

There are four separate comparator units terminated at a Quad Comparator CP-151 and CP-152.

Figure 2.8-1 shows the comparator patching area and a simplified schematic of one of the comparators. (The other comparators are identical.) The relay termination indicated by the negative sign is the position of the relay when the sum of the IN1 and IN2 input is negative, this is the de-energized position of the relay. When the sum of the IN1 and IN2 is positive, the relay energizes and the wiper swings to the positive contact.

(1) Comparator Switching Data of CP-151

Relay Switching Time

Typical ..... 5 milliseconds

Maximum allowable .....10 milliseconds

Sensitivity

Typical ..... 30 millivolts

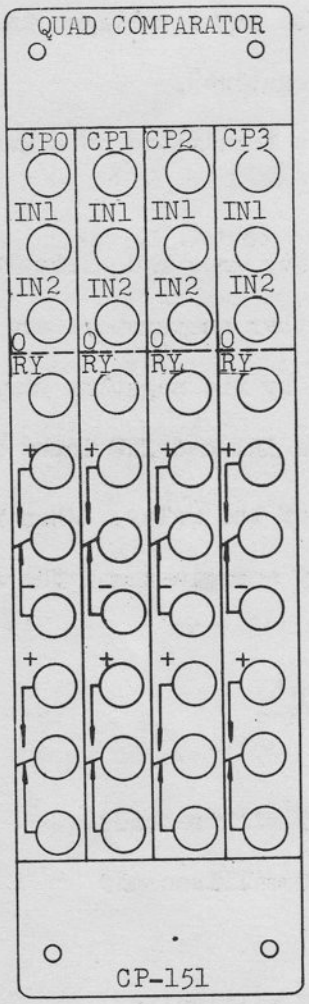
Minimum ..... 50 millivolts

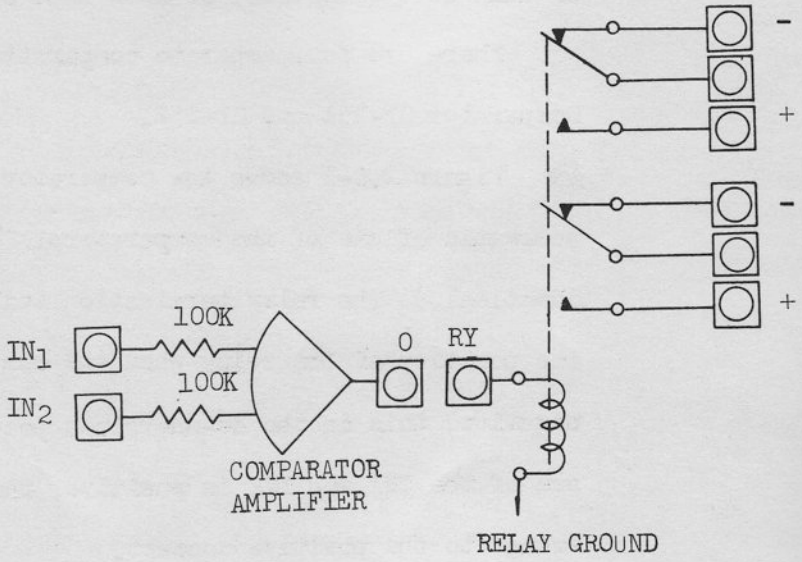
(2) Comparator Switching Data of CP-152

Relay Switching Time

Typical .....300 microseconds

Maximum allowable ..... 500 microseconds





NOTE: COMPARATOR RELAY SHOWN
DE-ENERGIZED

FIGURE 2.8-1 COMPARATOR PATCHING AREA AND SIMPLIFIED SCHEMATIC

Sensitivity

Typical ..... 30 millivolts

Minimum ..... 50 millivolts

Each model of the comparator has the voltage output which has switching time less than 10 microseconds. The output can drive the integrator mode and etc., directly.

(3) Set Up Procedure The problem variable that is to control the comparator switching should always be applied to the IN1 termination and the reference or bias voltage should be applied to the IN2 termination. The following is the set-up procedure for the comparator.

(a) Apply an input to the IN1 termination equal in magnitude and potarity to the desired switching level.

(b) Connect the wiper of a potentiometer to the IN2 termination; apply reference, opposite in polarity to the IN1 input, to the potentiometer high end.

(c) Adjust the input to IN2 so the comparator relay is actuated as required when IN1 reaches the switching level. (The output of each comparator can be selected to the selector system.)

(d) The comparator is now set for use in the problem and should be patched to the appropriate signal sources.

The steps mentioned above can be replaced by the adjusting of the bias potentiometer in the reset mode using the potentiometer selector system, if high accuracy is not required.

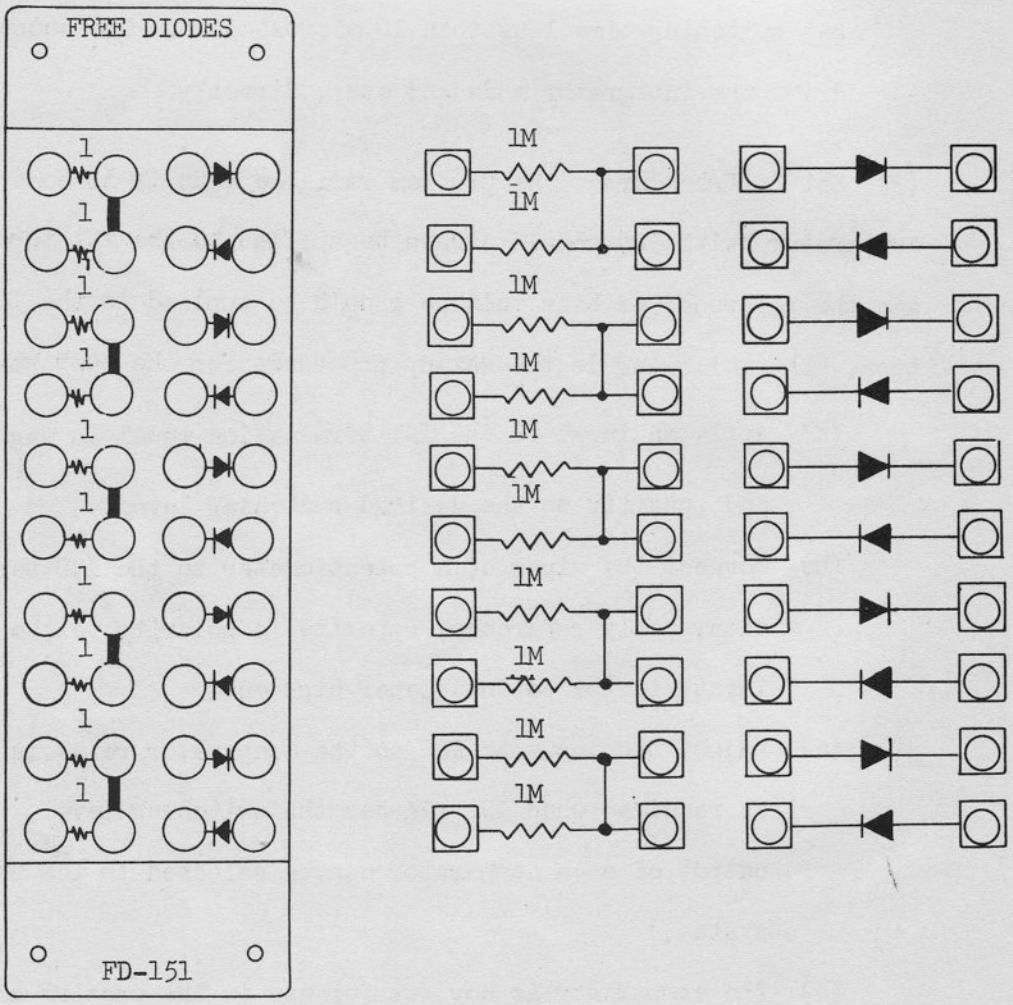


FIGURE 2.9-1 FREE DIODES PATCHING BLOCK AND SCHEMATIC

9. FREE DIODES FD-151

Many non-linear phenomena may be simulated by using the combination of resistors and diodes in the Free Fiodes FD-151 with the potentiometers. Applications will be shown in Appendix 7.

10. TRANSFER DELAY ELEMENT TD-151

The Transfer Delay Element TD-151 causes time delay by Pade's second order approximation. Two dc amplifiers (a DA-151 or equivalent) are necessary for the complete circuit as shown in Figure 2.10-1.

With two elements connected in series, the transfer delay given by Pade's fourth order approximation can be approximately produced. In this connection, the delay time will develop to the sum of the value set in two elements. Set a half or nearly a half of delay time on each element. For better simulation, the fourth order approximation will be recommended.

The Transfer Delay Element TD-151 has a wide range of delay time, but combination of both R and C which make the delay time T must be restricted by the viewpoint of simulating accuracy. The Table 2.10-1 will show a guide to select a combination of R and C.

The TD-151 can be used in both Real Time Operation (RT) and Repetive Operation (RO), and the connection of capacitors are automatically transfered in a same way to the Integrator, synchronizing to the Integrator Capacitor switch on the Control Panel.

INPUT MAXIMUM ANGULAR FREQUENCY ω	MAXIMUM DELAY TIME	MINIMUM DELAY TIME	CAPACITANCE TO BE USED
BETWEEN 0.1 - 1.0	11 SEC	0.1 SEC	1 MFD
1.0 - 10	1.1	0.01	0.1
10 - 100	0.11	0.001	0.01
100 - 1000	0.011	0.0001	0.001

NOTE: THE PRODUCT OF INPUT MAXIMUM FREQUENCY ω AND DELAY TIME T SHOULD NOT EXCEED 2, TO KEEP THE HEIGHT OF INITIAL TRANSIENT LESS THAN 10%.

THE SERIES CONNECTION OF TRANSFER DELAY TD-151 WILL MARK BETTER SIMULATION. IN CASE, DELAY TIME

IT SHOULD BE NOTED THAT OUTPUT SIGNAL POLARITY IS JUST OPPOSITE TO INPUT IN A SIGNLE TD-151 OPERATION.

TABLE 2.10-1 DELAY TIME SETTING TABLE

Set-Up Procedure

(a) Find the combination of R and C from the Table 2.10-1.

(b) Patch the above value on the Pre-Patch Panel.
The set value of R is the value which has not been shorted by the patchcords. An illustration is shown in Figure 2.10-2.

(c) Ascertain the function applying the input and watching the input and output on the oscilloscope if possible. This will reduce the difficulty in the analysis due to errors in patching or inadequate RC selection.

In the patching of the capacitor, the circled terminal in RT or RO area in the Pre-Patch Panel should be connected to the circled terminal in one of the capacitor area.

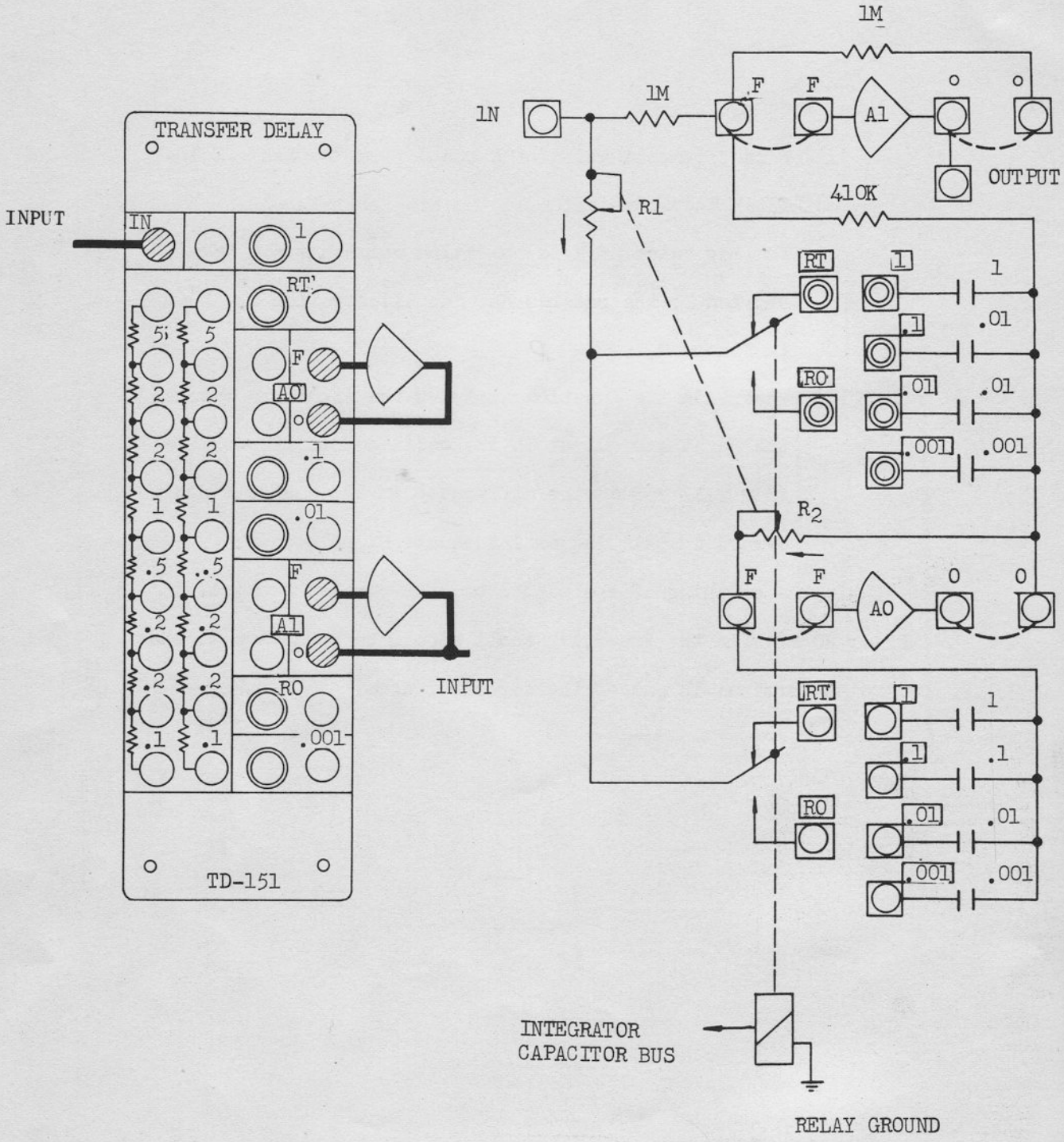
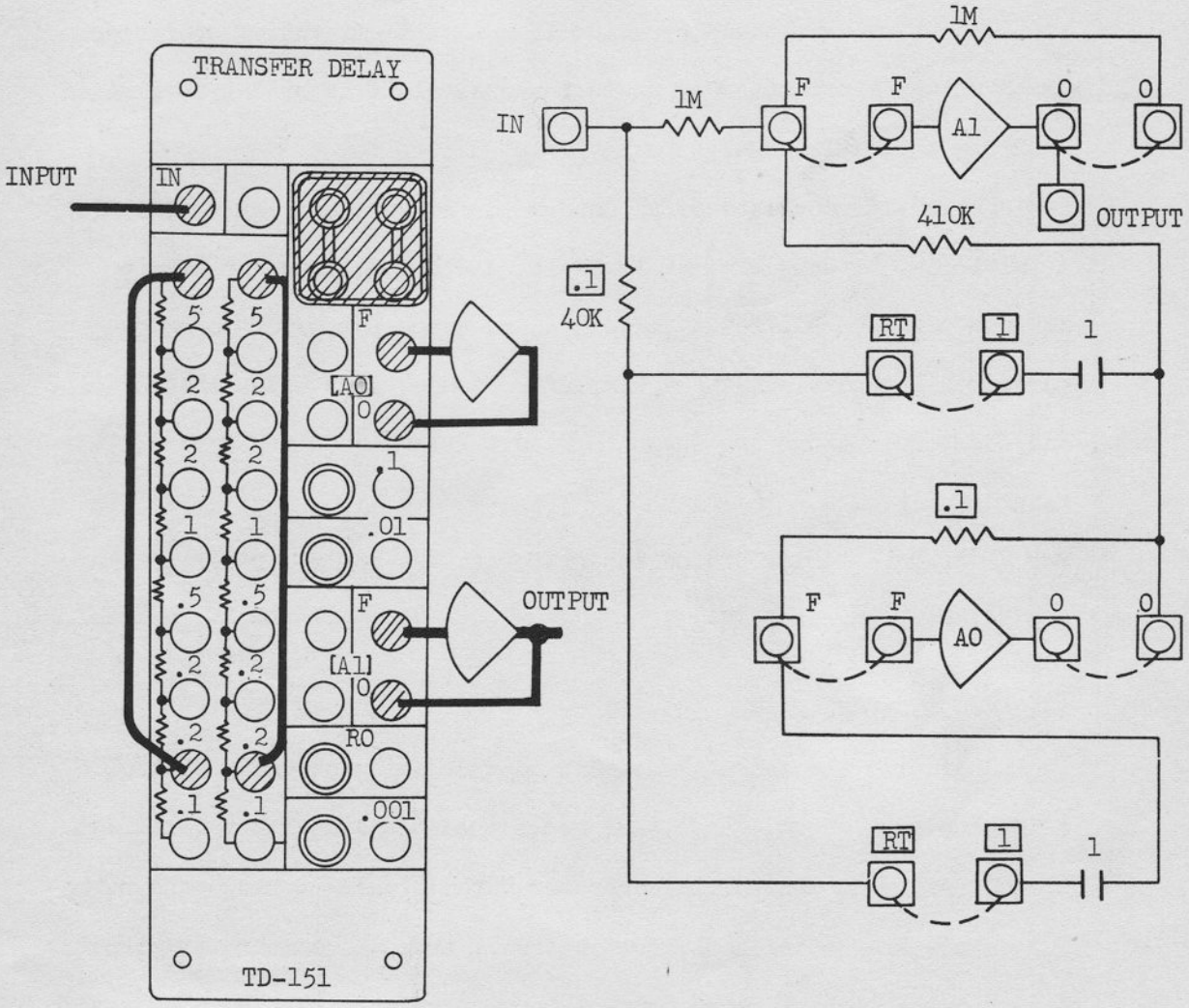


FIGURE 2.10-1 TRANSFER DELAY ELEMENT, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK LAYOUT



RELAY TIME 0.1 SEC SETTING
FOR RT OPERATION

FIGURE 2.10-2 TRANSFER DELAY ELEMENT TYPICAL PATCHING AND SIMPLIFIED SCHEMATIC

11. AUTOMATIC OPERATOR AO-151

The Automatic Operator AO-151 is a versatile device to determine an eigen value or a boundary value in automatic iterative operation, or to change a parameter by an incremental digit according to time in a simple repetitive operation.

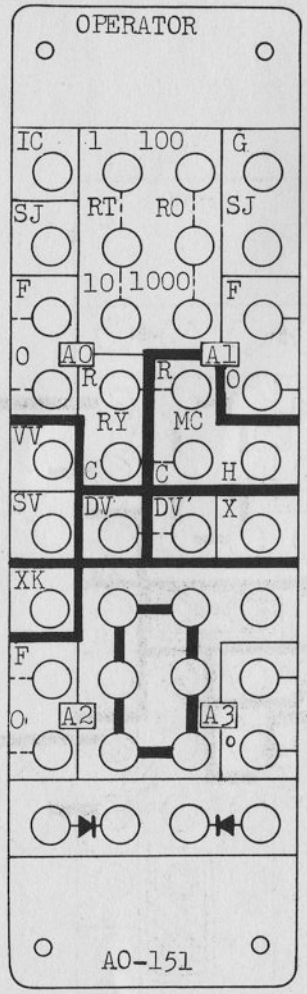
The AO-151 consists of an integrator network similar to IN-151, a multiplier network similar to EM-151 and a committed network to compose a feedback circuit to seek an adequate parameter to satisfy the circuit conditions. The simplified connections using the AO-151 and its terminations are shown in Figure 2.11-2 and in Figure 2.11-3 respectively.

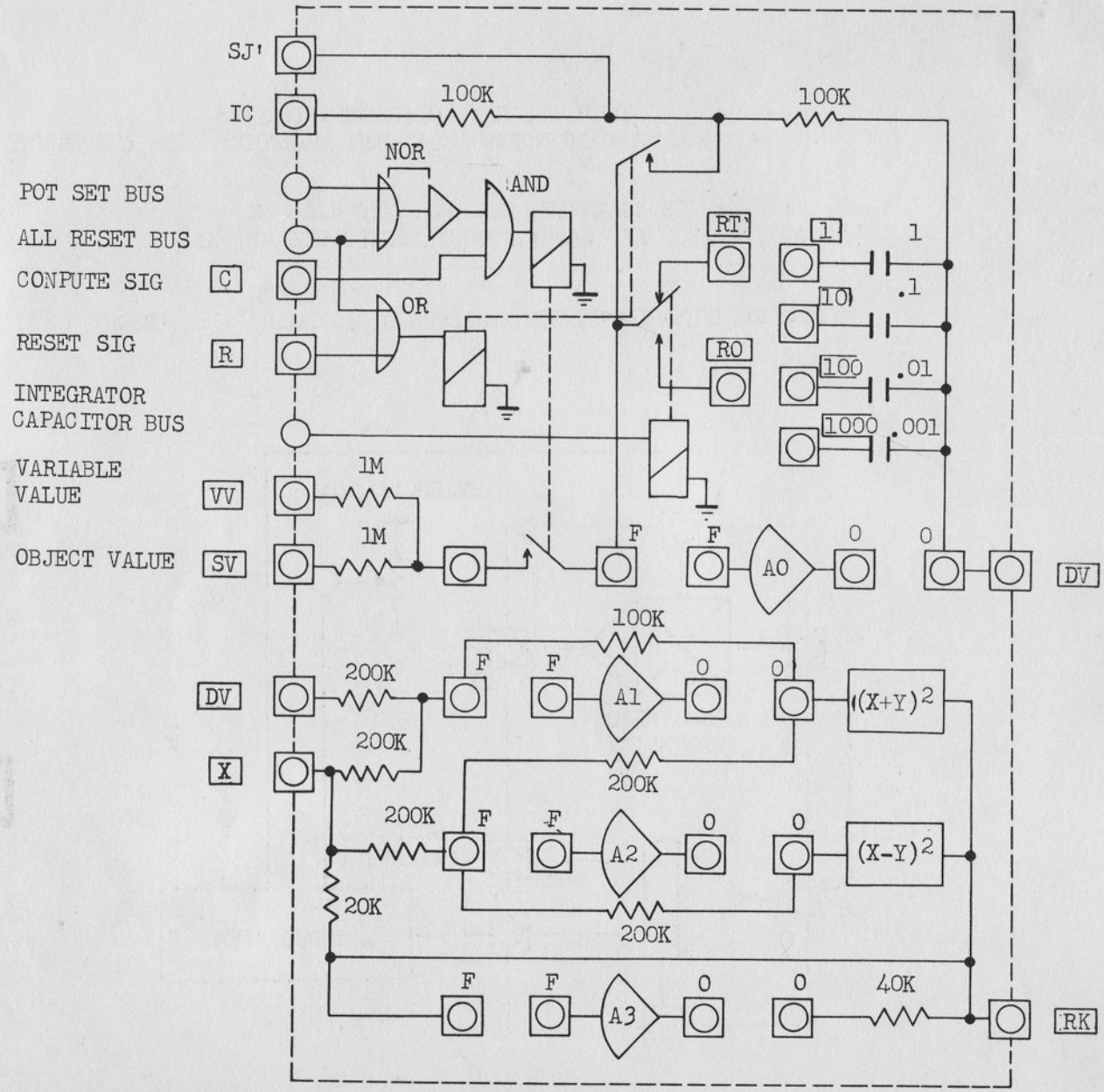
For the patching of the integrator in the AO-151, refer to the one of the Integrator IN-151.

12. MODE CONTROL PANEL MC-151

Ordinally the computer mode is controlled by the mode control switch on the Control Panel, and occasionally the operator will feel the necessity to control the computer automatically through the patching on the Pre-Patch Panel, for instance, from the comparator output. For this requirement, mode control input terminals have been prepared on the Mode Control Panel MC-151. The MC-151 supplies six input terminals: RESET (designated as RS), COMPUTE (CP), HOLD (HD), POT SET (PS), ALL RESET (AR) and REPETIVITIVE OPERATION (RO).

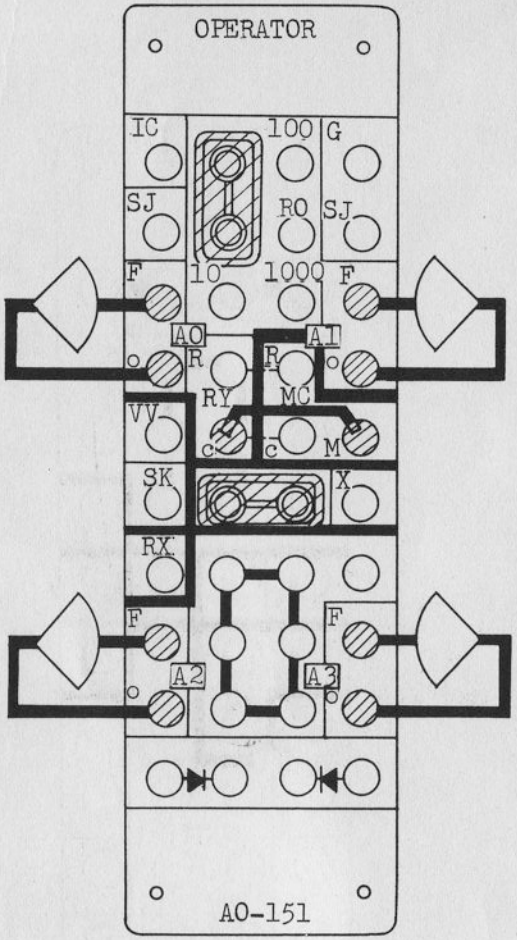
If the voltage 12 volts through 24 volts is applied to the terminal the computer mode will change just same as the mode control button is pushed.

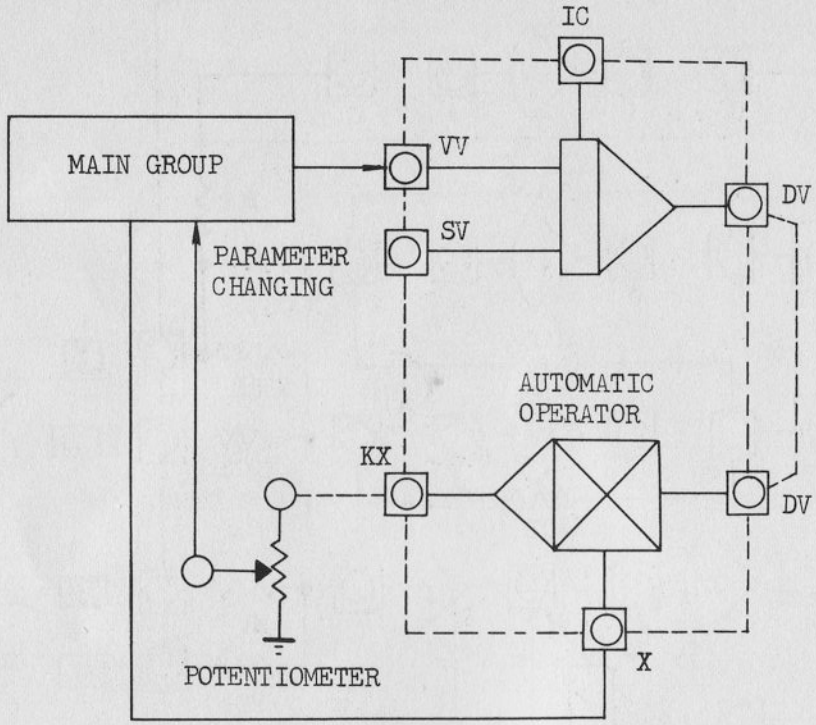




NOTE: AMPLIFIERS ARE NOT INCLUDED IN THE MODULE

FIGURE 2.11-1 AUTOMATIC OPERATOR, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK LAYOUT





NOTE: 1. AUTOMATIC OPERATOR OPERATES IN HOLD MODE OF MAIN GROUP.

2. IN THE CIRCUIT SHOWN ABOVE, VV CONVERTS TO SV WITH CHANGING THE PARAMETER K.

FIGURE 2.11-2 AUTOMATIC OPERATOR, BLOCK DIAGRAM FOR TYPICAL CONNECTION AND PATCHING

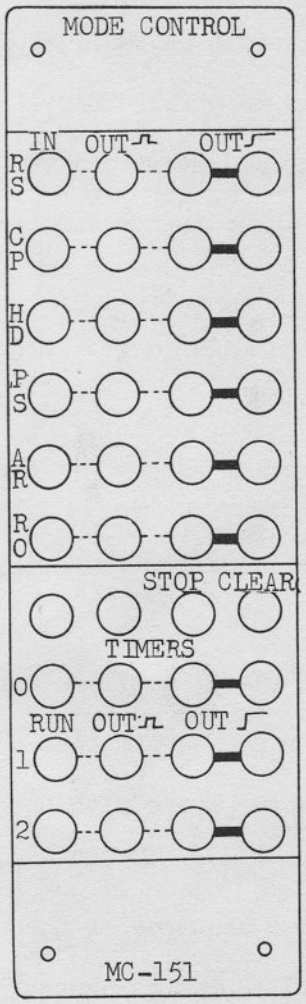


FIGURE 2.12-1 MODE CONTROL PANEL PATCHING BLOCK LAYOUT

The priority between signals is the same to the relation in the mode control buttons, that is;

(1) Pot Set has the first priority

(2) All the modes are divided into the groups.

A group consists of RESET, COMPUTE and HOLD, and another group consists of POT SET, ALL RESET and REP OP. The operator should first add the RESET signal when he wishes to change the computer mode from the second group to the first.

The output of the mode control signals are terminated on the same panel in the shapes of the pulse and the step function. They will be used as a special purpose integrator mode control or inputs to the timers which terminate on the same patching area.

TIMERS

The Timer Panel TM-251 supplies three timers which can be operated independently or in a series combination. On the Timer Panel, three timers occupy the center space with three pairs of the time setting dials, and above them there are three pairs of indicator neon lamp which will inform time sequence of the each timer operation. These timers can be controlled by the control buttons on the Timer Panel or signals from both the Mode Control Panel MC-151 on the analog Pre-Patch Panel and the Ring Counter RC-151 on the logic control panel. The Timer Panel is shown in Figure 2.13-1.

In the state that the toggle switch in the control area of the TM-251 turns to SINGLE side, each timer operates independently and supplies the output signal for the period adjusted with two dials; the TIME dial and the MULTIPLIER dial.

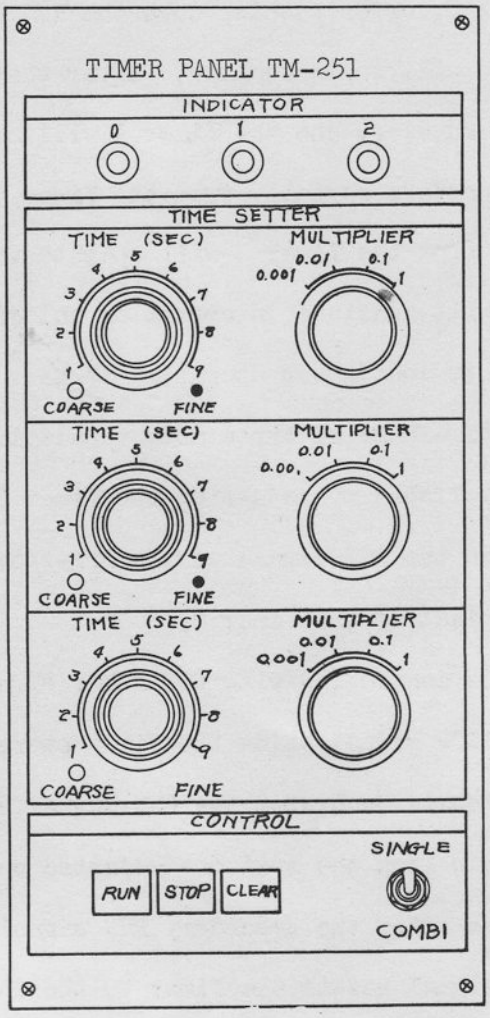


FIGURE 2.13-1 TIMER PANEL TM-251

In the state that the toggle switch mentioned above turns to COMB1 side, these timers will operate in series combination repetitively. In this state, when the signal (12 volts through 24 volts) is applied to the input of the Timer 0, or by pushing down the RUN button on the CONTROL area, the Timer 0 will begin running. After the adjusted period, the Timer 0 will stop running, and the Timer 1 will begin operating. Thus the operation transfers serially from the Timer 0 through the Timer 2, and the end signal from the Timer 2 will operate the Timer 0. The loop of three timers will continue in operation unless STOP or CLEAR SIGNAL is Applied. This continuous operation is very usefull to allow the operation of the time base of three mode repetitive or iterative operation can be accomplished by adjusting the Timer 3 setting to zero. In the serial operation the RUN signal on the Pre-Patch Panel should be applied on the IN terminal of the Timer 0.

The Timer Panel is controlled with two other signals;
STOP and CLEAR: The STOP signal holds the Timer operation momentary in series combination state, and when the RUN signal applied, the Timer will operate again from the next one adjusted on the panel. Note that the operation time after the secondary RUN signal is independent to the time the STOP signal resets the Timer to the initial state. Detailed operation is explained on Figure 2.13-1.

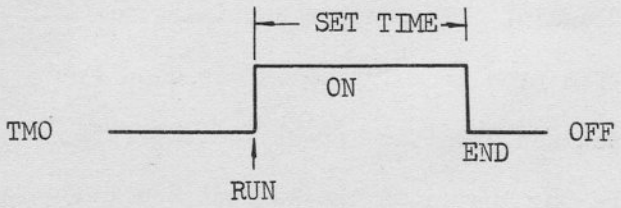
The Timer Panel TM-253 is prepared to supply the simple time base used in the REP OP button on the Control Panel is pushed. The REP OP signal from the TM-253 will be supplied to the electronic mode control sequence in the Control Panel.

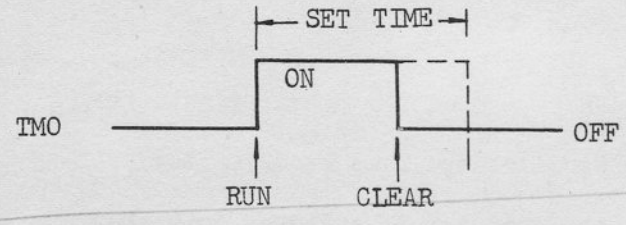
Essentially, the Rep-Op mode, with the time scaling and rapid switching between the integrator reset and the compute modes, a problem

1. SINGLE OPERATION

REMARK:
"PULSE-OUTPUT" GIVES AT THE BEGINNING OF EVERY TIME-PERIOD A SHORT PULSE (2 μSEC'S, AS LOGICAL "1")

EACH TIMER OPERATES INDEPENDENTLY FROM OTHERS WITH "RUN" SIGNAL. TIMER GENERATES "ON" SIGNAL FOR THE PERIOD OF SET TIME.

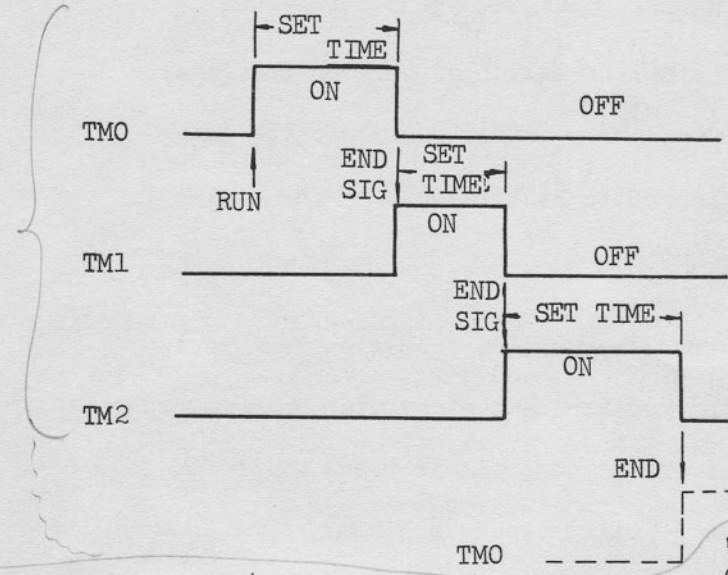




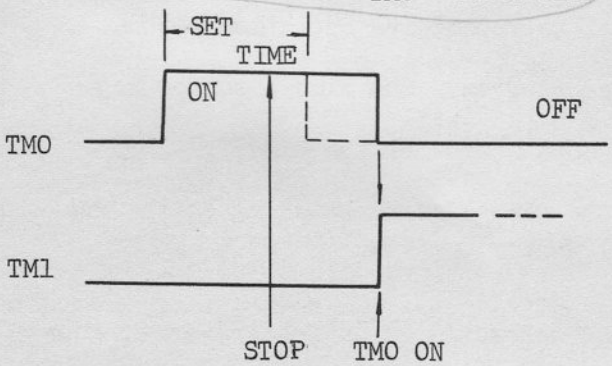
"CLEAR" SIGNAL IN OPERATION PERIOD MAKES TIMER OPERATION OFF.
"STOP" SIGNAL DOES NOT ACTUATE IN SINGLE OPERATION.

2. GROUP (COMBINATION) OPERATION

IN GROUP OPERATION, "END" SIGNAL RUNS NEXT TIMER, AND THE LAST TIMER RUNS THE FIRST TIMER. THUS THREE TIMERS OPERATE SERIALLY UNLESS "STOP" OR "CLEAR" SIGNAL IS APPLIED.



"RUN" SIGNAL SHOULD BE APPLIED TO TMO IN THIS GROUP OPERATION.



"STOP" SIGNAL IN A TIMER OPERATION POSTPONES THE TIMER OPERATION TO THE TIME TMO "ON" SIGNAL WILL BE APPLIED.

CONTINUOUS "STOP" AND TMO "ON" SIGNALS WITHIN AN OPERATION TIME OF A TIMER WILL NOT AFFECT THE TIMER OPERATES THEN AS IF NO SIGNAL IS ADDED.

FIGURE 2.13-2 TIMER OPERATION

is solved, reset, and then solved again, this process continues repetitively at the pre-set rate. The problem solution may be displayed on an oscilloscope that is synchronized with the Rep-OP cycling rate. The inputs to the Oscilloscope are terminated on the Readout Panel OC-151.

To place the computer in the Rep-Op mode the operator sets the desired rate on the timer or the Oscilloscope Time Base. After setting the desired repetition rate, the computer is switched into the Rep-Op mode by depressing the REP OP button on the control panel.

Mind that the Integrator Capacitor switch on the Control Panel should be turned to RO if the operator require to operate the integrators with the capacitor connected to RO terminal.

14. REPETITIVE OPERATION

The addition of the high-speed repetitive operation feature to the 505 provides means of rapidly switching the computer integrators between the RESET and COMPUTE modes at controlable rates up to 50 cycles per second (compute time 10 milliseconds minimum). The computer can be switched from manual to repetitive operation without requiring changes to the computer program. The time base for Rep-Op is supplied from the Oscilloscope OS-251 or the Timer TM-253. The Timer TM-251 also supplies the time base by patching on the Pre-Patch Panel.

Figure 2.5-5 is a simplified schematic of an integrator showing the Rep-Op capacitors and the Time Scale relay. Energizing the Time Scale relay K1, the feedback capacitor is changed from the capacitor connected to the RT terminal to the capacitor connected to the RO

terminal, thus changing the integrator time scaling by a factor, one of 10, 100 and 1000. The time scaling of each integrator can be decided arbitrary, the operator can use iterative techniques in problem solution by operating desired integrators at "real time" rates even though the computer is in the Rep-Op mode.

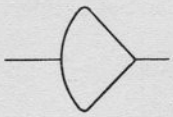
The Time Scale Relay is controlled with the Integrator Capacitor Switch, therefore, the low speed Rep-Op can be accomplished if an adequate timing signal is supplied to the Control Panel through the Pre-Patch Panel.

Essentially, the Rep-Op mode, with the time scaling and rapid switching between the integrator reset and the compute modes, means that a problem is solved, reset, and then solved again, this process continues repetitively at the pre-set rate. The problem solution may be displayed on an oscilloscope that is synchronized with the Rep-Op cycling rate. The inputs to the Oscilloscope are terminated on the Readout Panel OC-151.

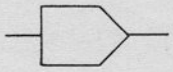
To place the computer in the Rep-Op mode the operator sets the desired rate on the Timer or the Oscilloscope Time Base. After setting the desired repetition rate, the computer is switched into the Rep-Op mode by depressing the REP OP button on the control panel.

Remember that the Integrator Capacitor switch on the Control Panel should be turned to RO if the operator requires operating the integrator with the capacitor connected to RO terminal.

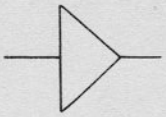
APPENDIX 1 COMPUTER SYMBOLS



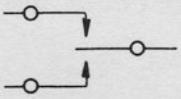
HIGH GAIN AMPLIFIER
(OPERATIONAL AMPLIFIER)



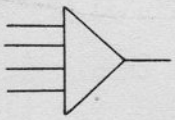
DIODE FUNCTION GENERATOR,
FIXED AND VARIABLE



INVERTING AMPLIFIER

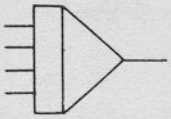


FUNCTION SWITCH



SUMMING AMPLIFIER

SOLID-STATE DIODE

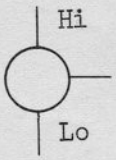


INTEGRATING AMPLIFIER

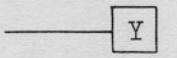
FIXED RESISTOR

HAND-SET POTENTIOMETER,
GROUNDED

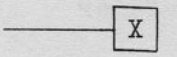
CAPACITOR



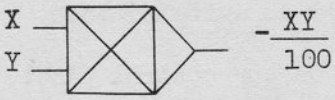
HAND-SET POTENTIO-
METER, UNGROUNDED



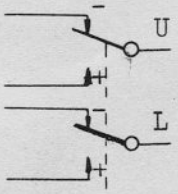
Y INPUT OF XY PLOTTER



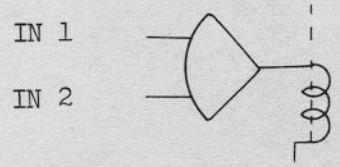
X INPUT OF XY PLOTTER



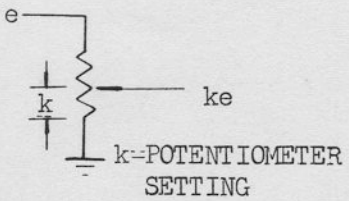
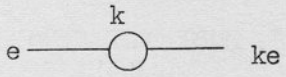
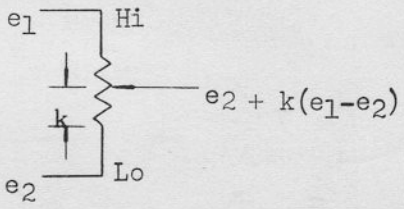
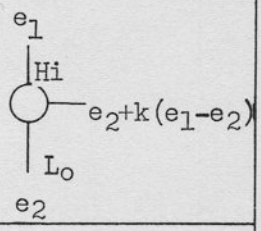
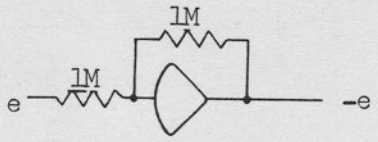
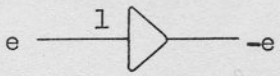
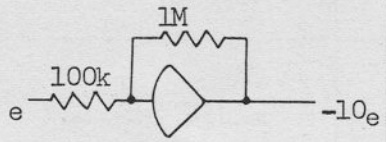
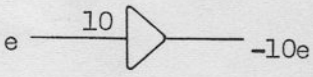
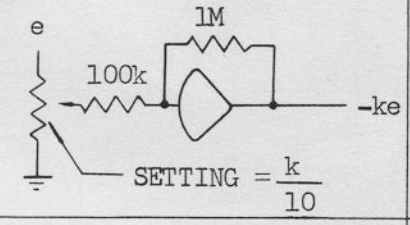
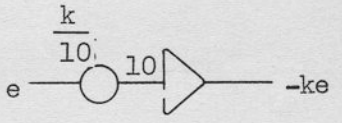
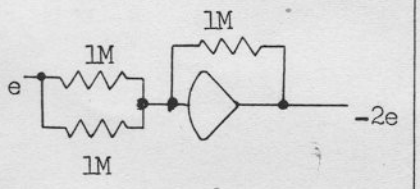
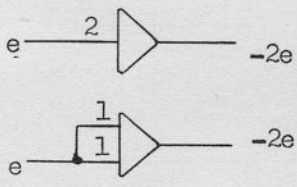
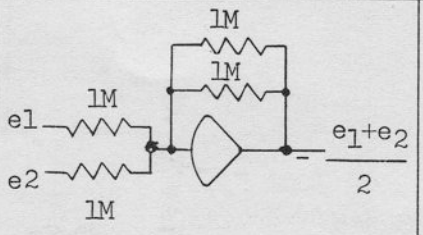
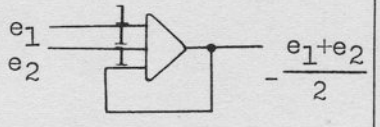
QUARTER-SQUARE MULTIPLIER,
MULTIPLICATION MODE



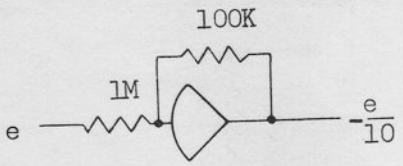
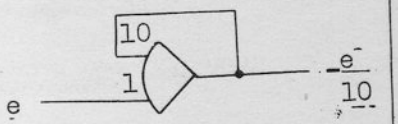
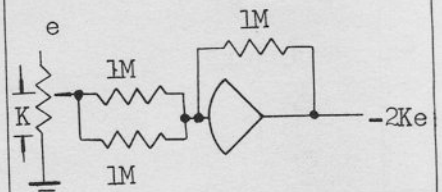
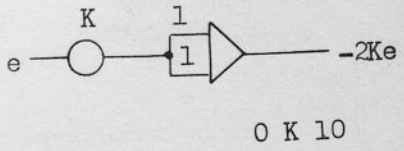
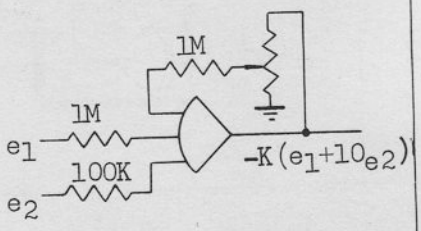
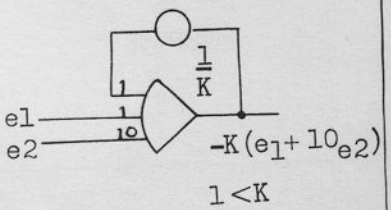
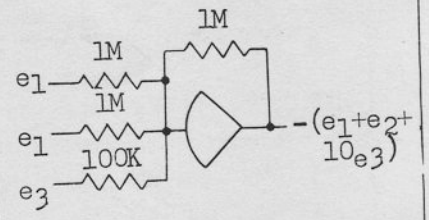
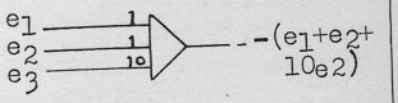
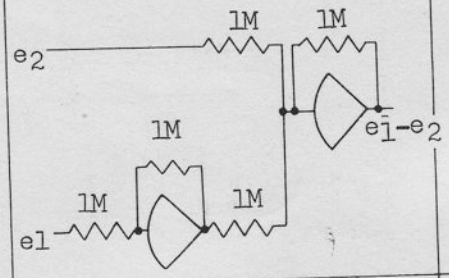
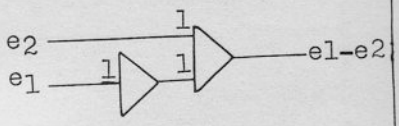
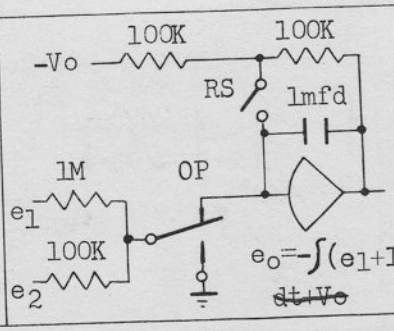
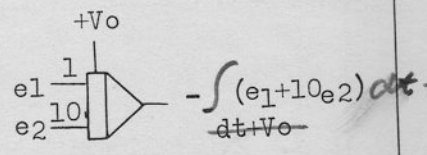
RELAY COMPARATOR



APPENDIX 2 SIMPLE CIRCUITS USING AMPLIFIER AND POTENTIOMETER

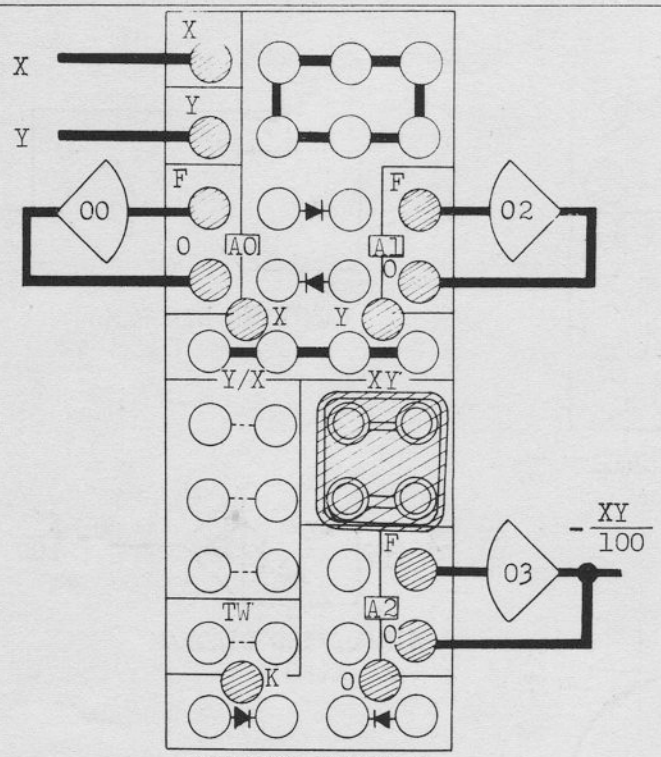
CIRCUIT DESCRIPTION	CIRCUIT	COMPUTER SYMBOL
1. GROUNDED POTENTIOMETER		
2. UNGROUNDED POTENTIOMETER		
3. INVERTER		
4. MULTIPLICATION BY -10		
5. MULTIPLICATION BY -k for $1 \leq k \leq 10$ (for $k<1$, use circuit 1 feeding circuit 3)		
6. MULTIPLICATION BY 2		
7. MULTIPLICATION BY $\frac{1}{2}$		

APPENDIX 2

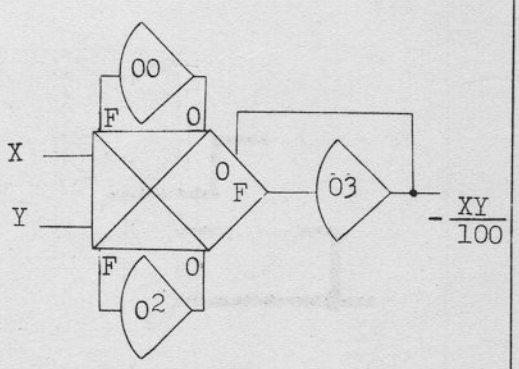
CIRCUIT DESCRIPTION	CIRCUIT	COMPUTER SYMBOL
8. MULTIPLICATION BY 1/10		
9. MULTIPLICATION BY AN ARBITRARY VALUE		
		
10. ADDITION		
11. SUBTRACTION		
12. INTEGRATION		

APPENDIX 3 MULTIPLIER CIRCUIT

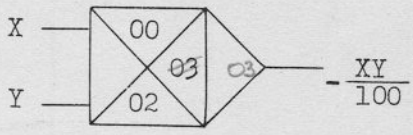
1. MULTIPLICATION



PATCHING DIAGRAM

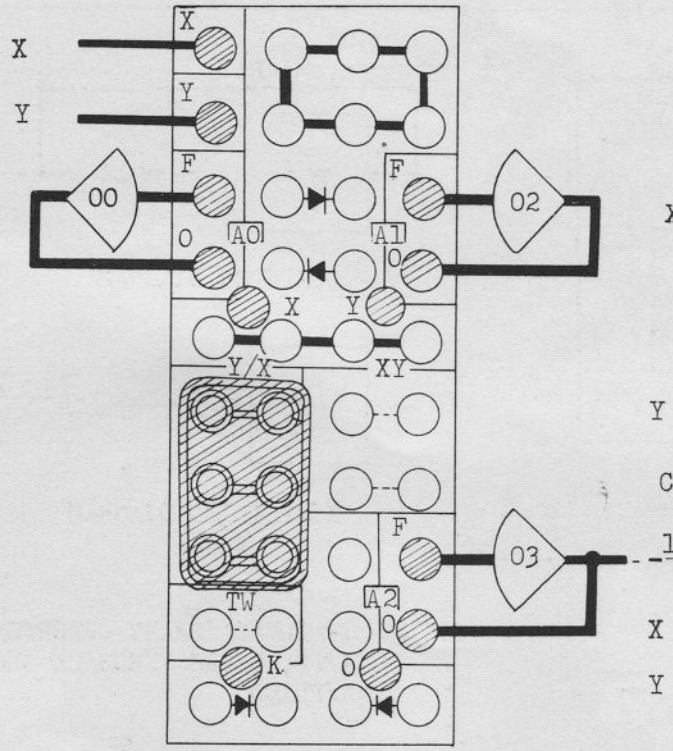


COMPUTER DIAGRAM

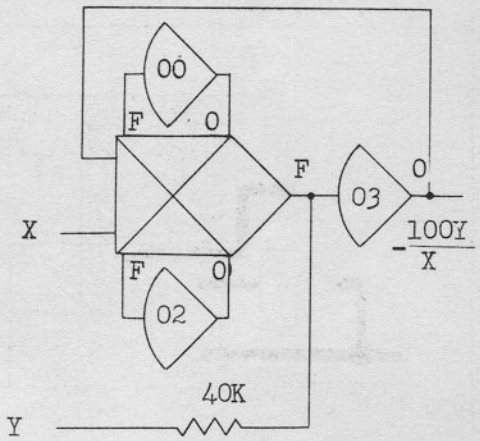


SIMPLIFIED DIAGRAM

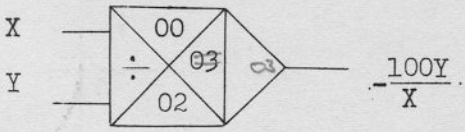
2. DIVISION



PATCHING DIAGRAM

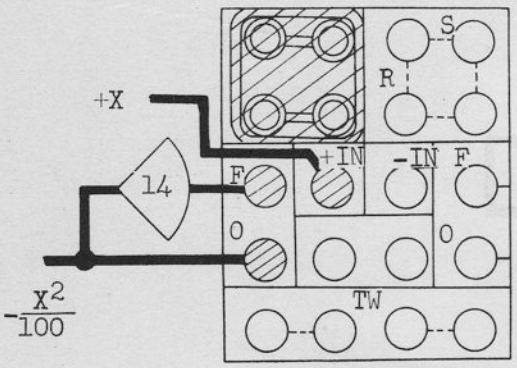


COMPUTER DIAGRAM

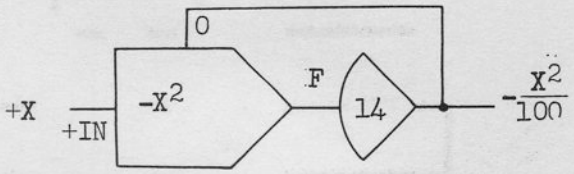


SIMPLIFIED DIAGRAM

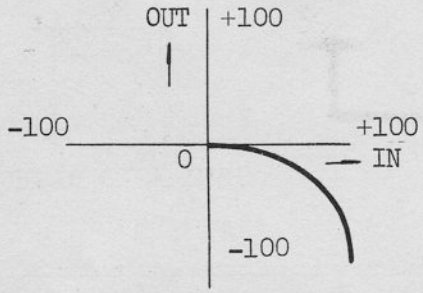
1. $-X^2/100$

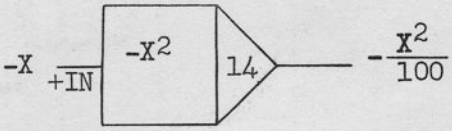


PATCHING DIAGRAM



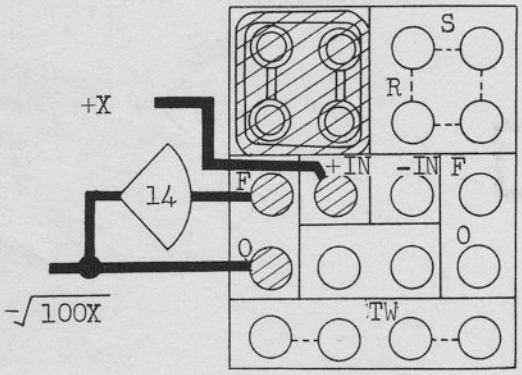
COMPUTER DIAGRAM



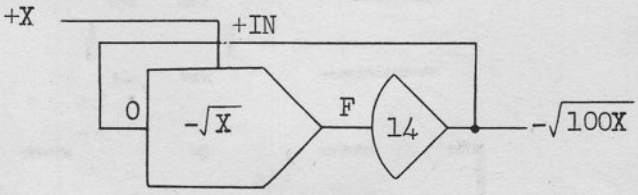


SIMPLIFIED DIAGRAM
$X > 0$

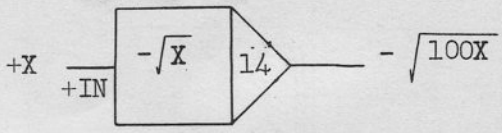
2. $-\sqrt{100X}$



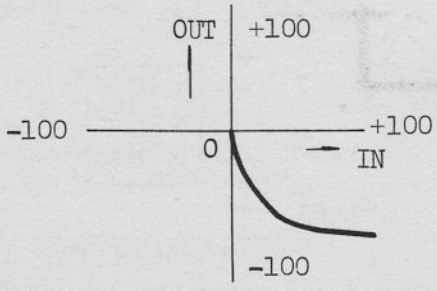
PATCHING DIAGRAM



COMPUTER DIAGRAM



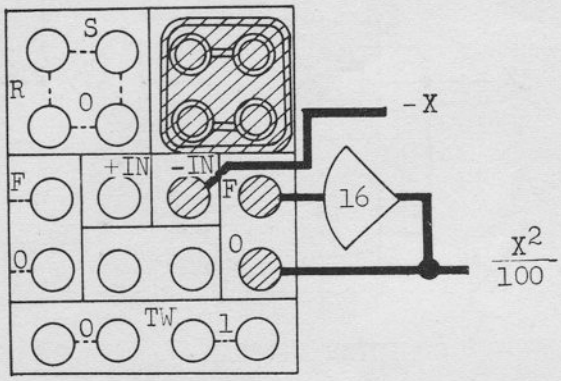
XIMPLIFIED DIAGRAM
$X > 0$



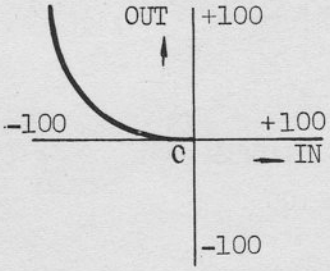
NOTE: IF THERE IS ANY OPPORTUNITY OF $X \leq 0$, DIODE FEEDBACK SHOULD BE APPLIED.

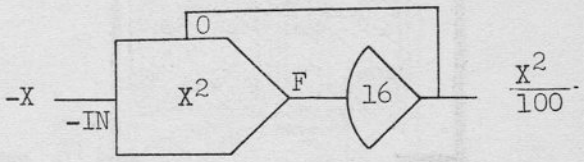
APPENSIX 4

3. $X^2/100$

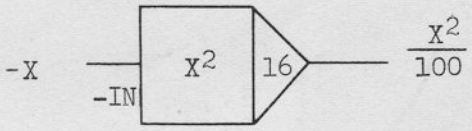


PATCHING DIAGRAM





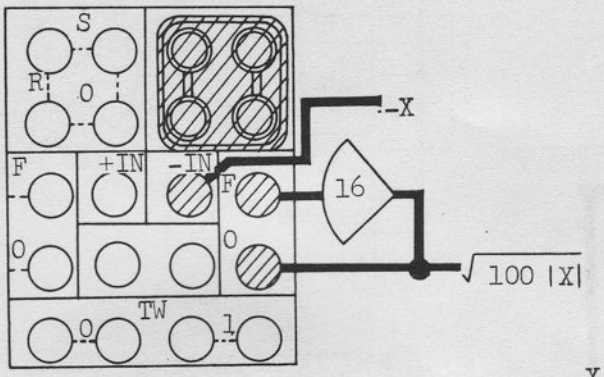
COMPUTER DIAGRAM



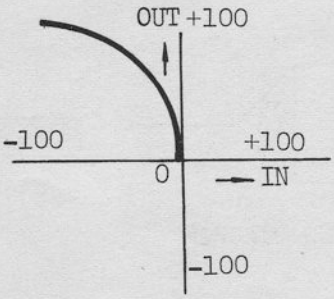
SIMPLIFIED DIAGRAM

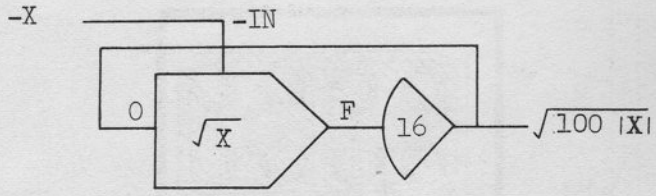
$-X < 0$

4. $\sqrt{100\ |X|}$

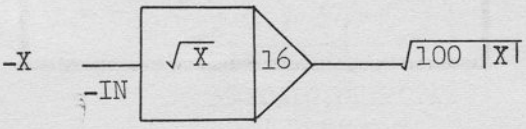


PATCHING DIAGRAM





COMPUTER DIAGRAM



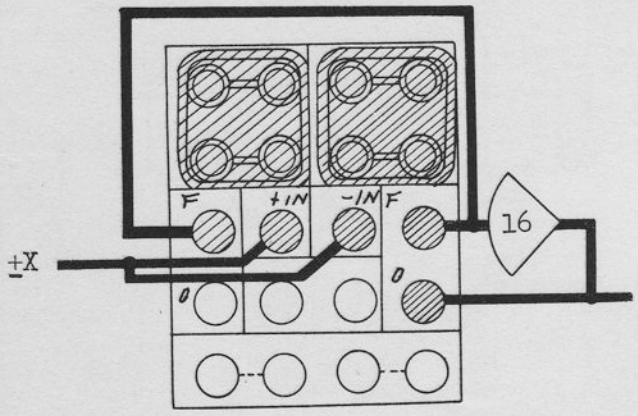
SIMPLIFIED DIAGRAM

$-X < 0$

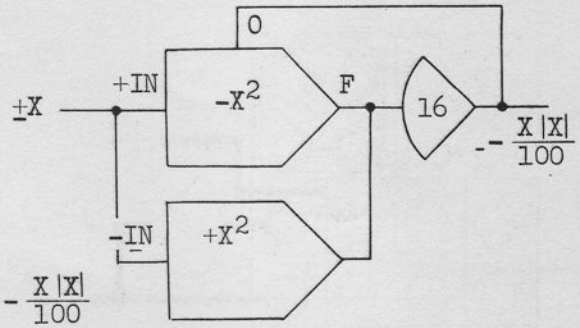
NOTE: IF THERE IS ANY OPPORTUNITY OF $X \leq 0$, DIODE FEEDBACK SHOULD BE APPLIED.

APPENDIX 4

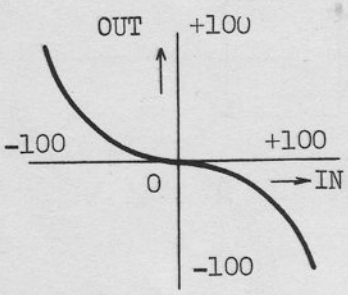
5. $X|X|/100$

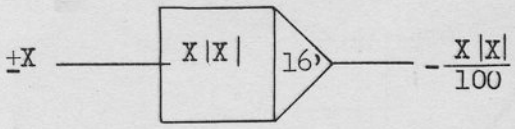


PATCHING DIAGRAM



COMPUTER DIAGRAM

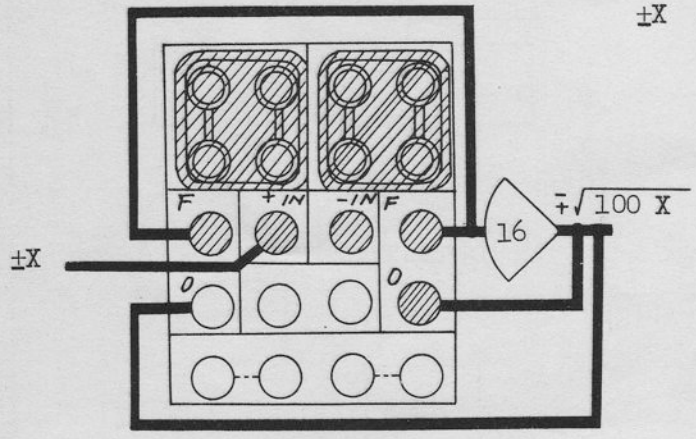




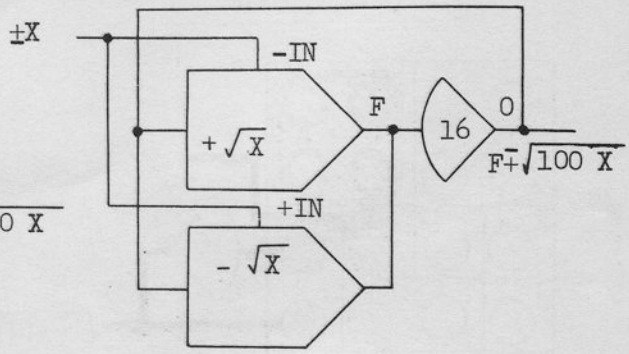
SIMPLIFIED DIAGRAM

$-100 \leq X \leq 100$

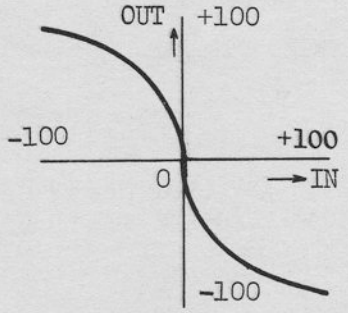
6. $\mp\sqrt{100\ X}$

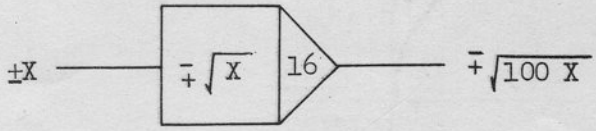


PATCHING DIAGRAM



COMPUTER DIAGRAM



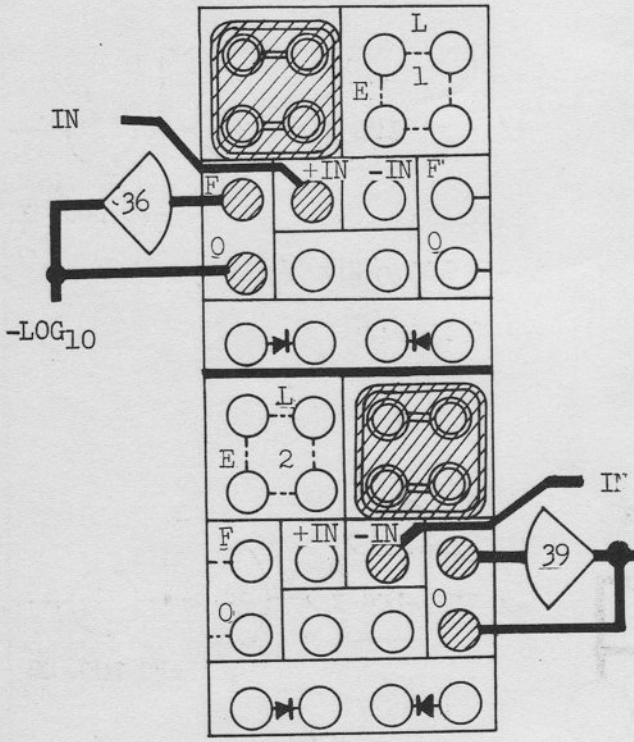


SIMPLIFIED DIAGRAM

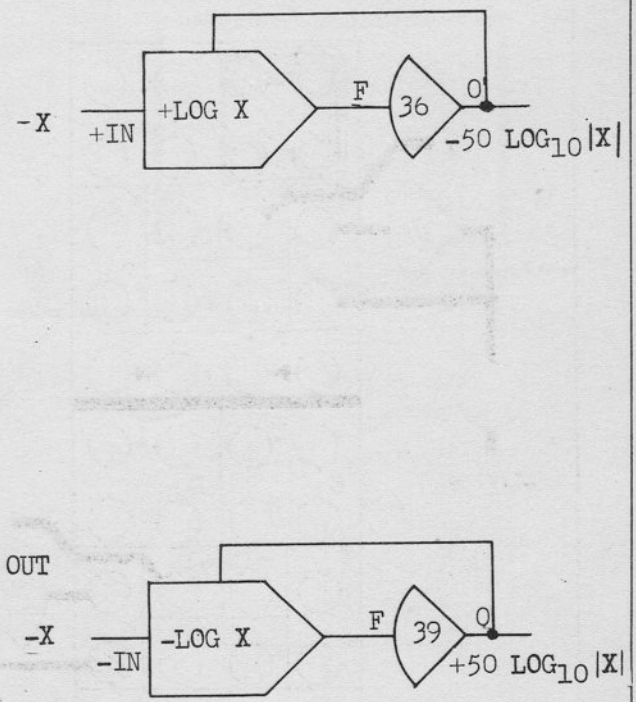
$-100 \leq X \leq 100$

APPENDIX 5 LOG X FG CIRCUITS

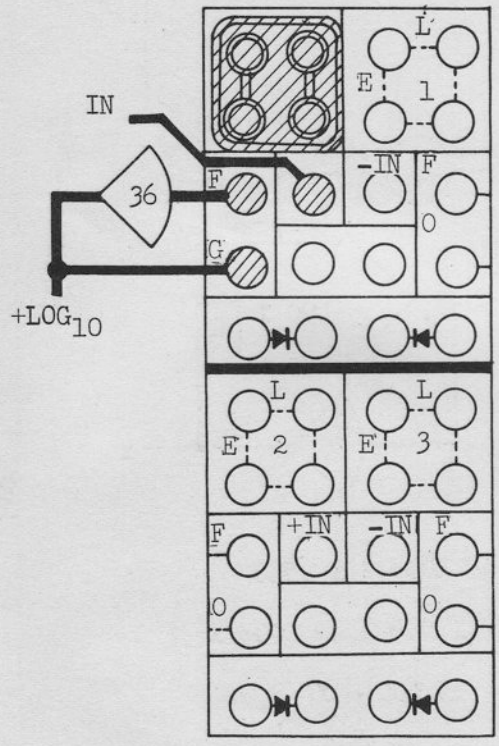
1. $LOG_{10}X$ FOR + INPUT AND + $LOG_{10}X$ FOR -X INPUT



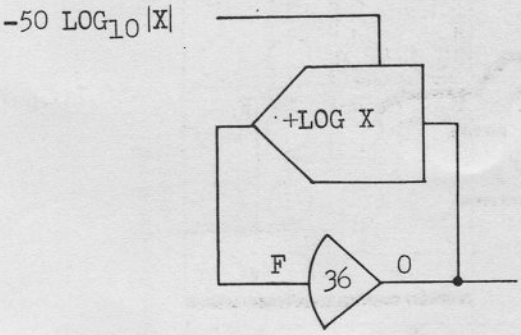
PATCHING DIAGRAM



2. ANTILOG, BASE 10



PATCHING DIAGRAM



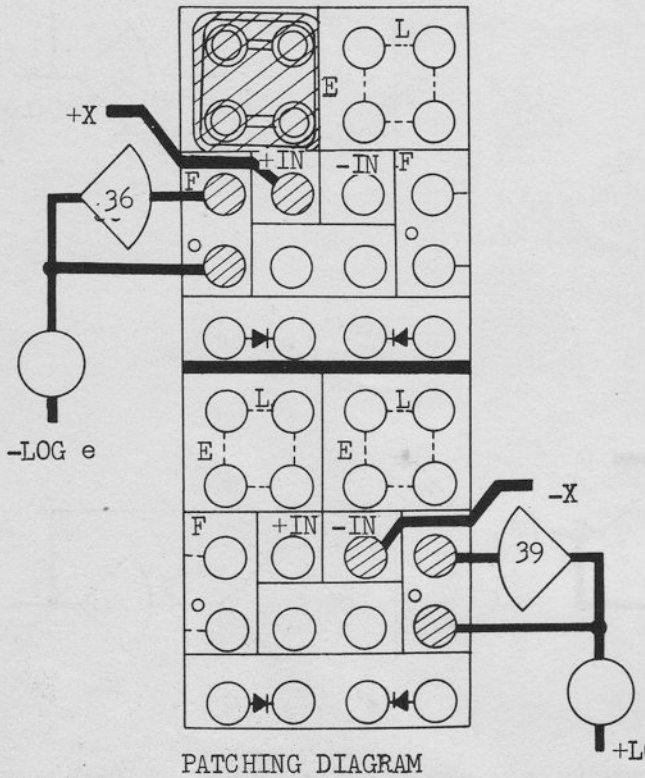
$$\text{LOG}\ \frac{-1}{10}\ \frac{1}{50}\left[\ 50\ \text{LOG}_{10}|X|\right] = X$$

$$0 < X \leq \pm 100$$

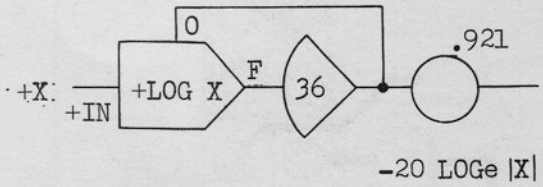
$$-100 \leq -50\ \text{LOG}_{10}|X| \leq 0$$

APPENDIX 5

3. LOG BASE e

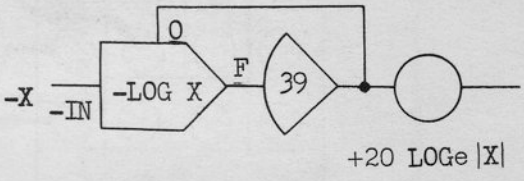


PATCHING DIAGRAM

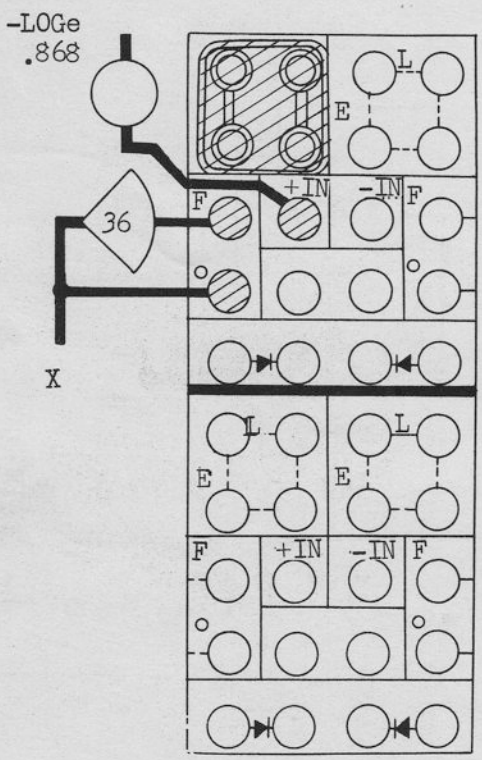


$\because -50 \text{ LOG}_{10}|X| \times .921$

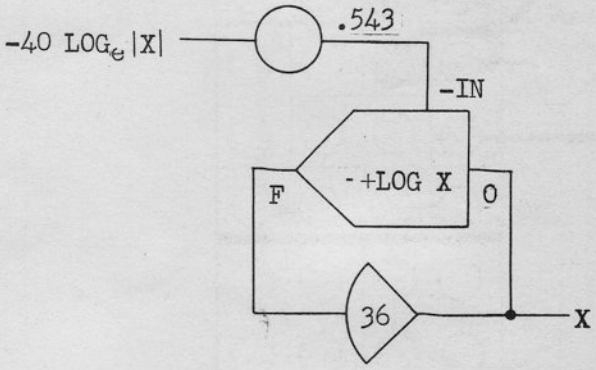
$= -20 \text{ LOGe}|X|$



4. ANTILOG BASE e



PATCHING DIAGRAM



$40 \text{ LOGe}|X| \times .543$

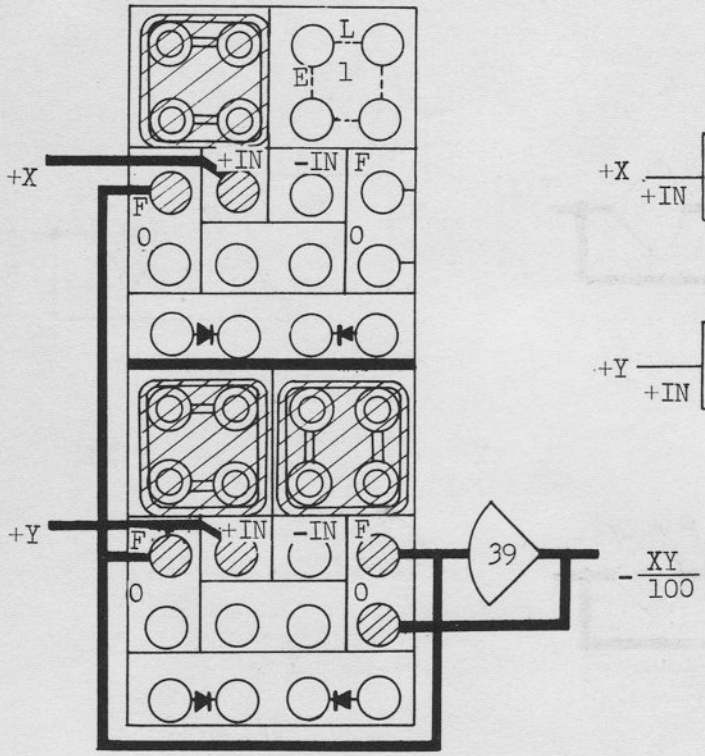
$= 1.086 \times 20 \text{ LOGe}|X|$

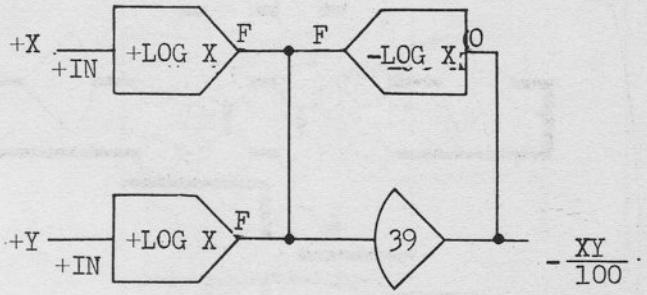
$= 50 \text{ LOG}_{10}|X|$

$\text{LOG}^{-1}_{10}\frac{1}{50}\left(50 \text{ LOG}_{10}|X|\right) = X$

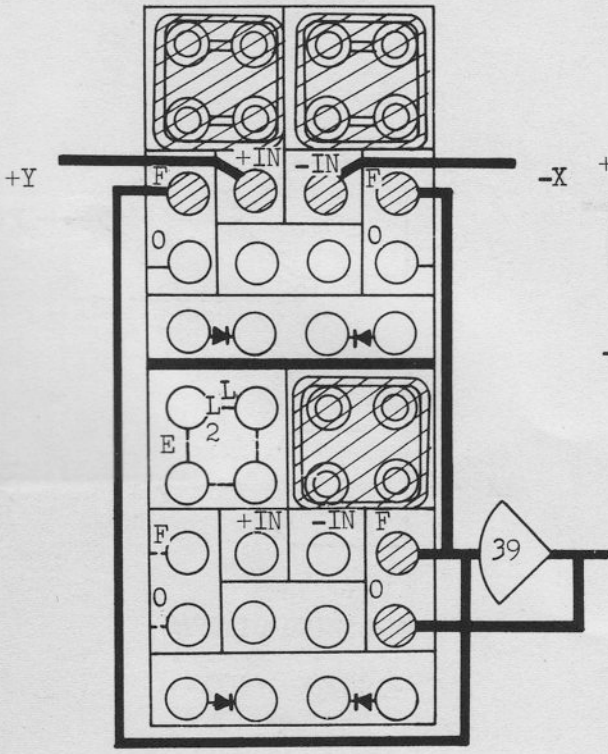
APPENDIX 5

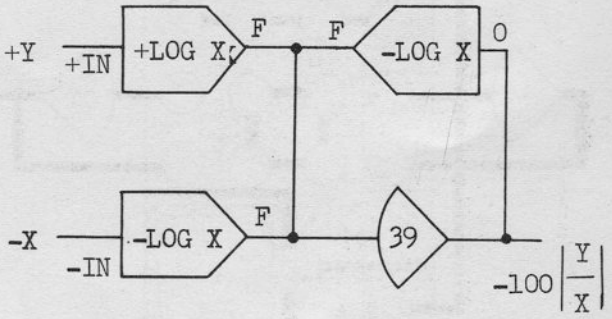
5. MULTIPLICATION (TWO VARIABLES) USING FG-155



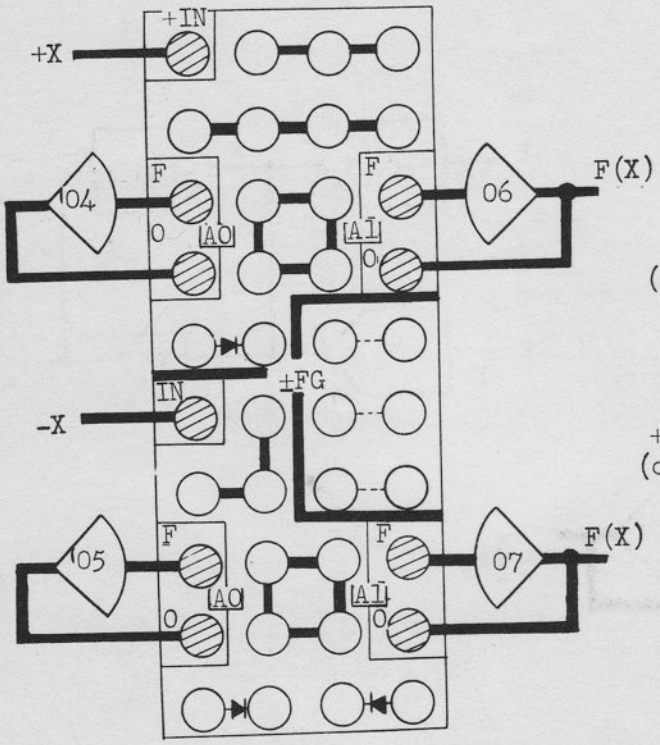


6. DIVISION (TWO VARIABLES)) USING FG-155

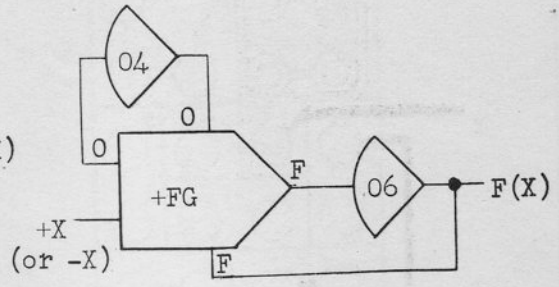




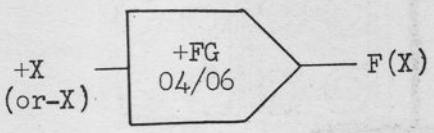
1. +VFG AND -VFG



PATCHING DIAGRAM



COMPUTER DIAGRAM



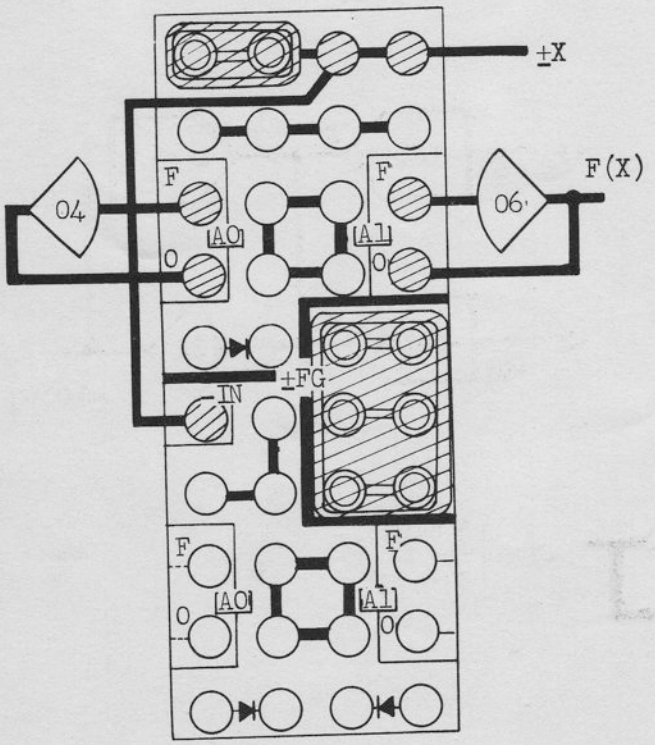
SIMPLIFIED DIAGRAM

$0 \leq X \leq +100$
or $-100 \leq X \leq 0$

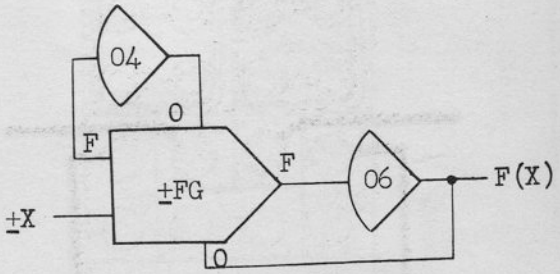
$-100 \leq F(X) \leq +100$

THE ABOVE DIAGRAMS SHOW POSITIVE INPUT CIRCUIT

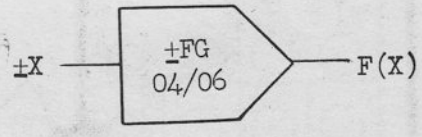
2. ±VFG (20 BREAK POINT)



PATCHING DIAGRAM



COMPUTER DIAGRAM



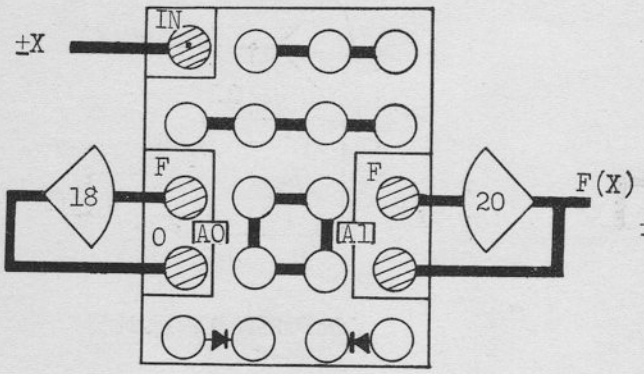
SIMPLIFIED DIAGRAM

$-100 \leq X \leq +100$

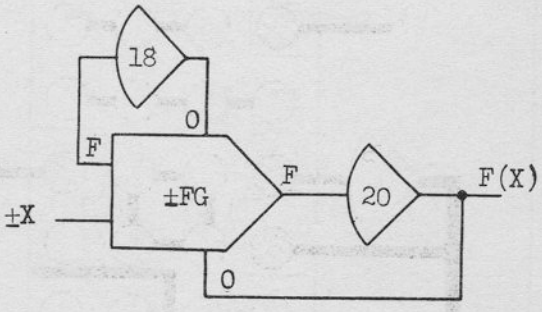
$-100 \leq F(X) \leq +100$

APPENDIX 6

3. ±VFG (10 BREAK POINT)



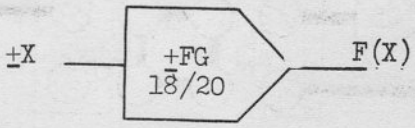
PATCHING DIAGRAM



COMPUTER DIAGRAM

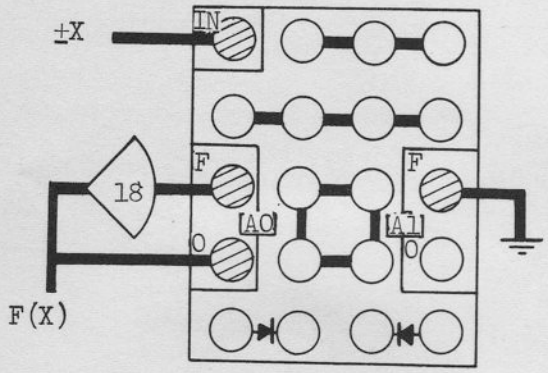
$-100 \leq x \leq +100$

$-100 \leq F(X) \leq +100$

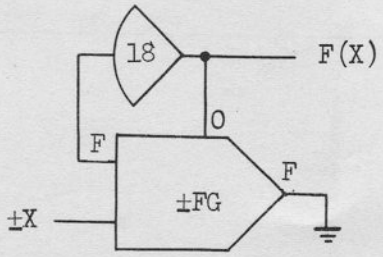


SIMPLIFIED DIAGRAM

4. ±VFG (10 BREAK POINT, MONOTONOUS FUNCTION)



PATCHING DIAGRAM

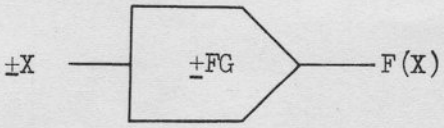


COMPUTER DIAGRAM

$-100 \leq X \leq +100$

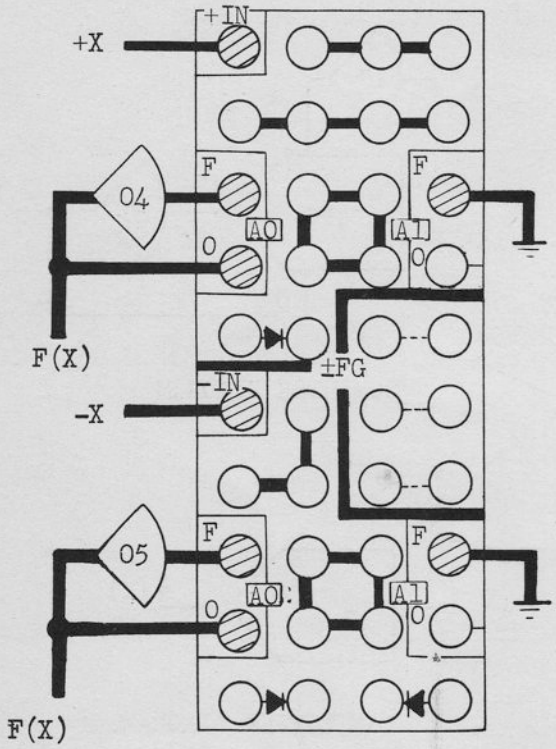
$-100 \leq F(X) \leq +100$

F(X): MONOTONOUS DECREASING FUNCTION



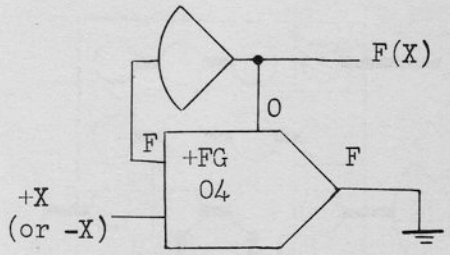
SIMPLIFIED DIAGRAM

5. +VFG AND -VFG (10 BREAK POINT, MONOTONOUS FUNCTION)



PATCHING DIAGRAM

F(X) : MONOTONOUS DECREASING FUNCTION



COMPUTER DIAGRAM

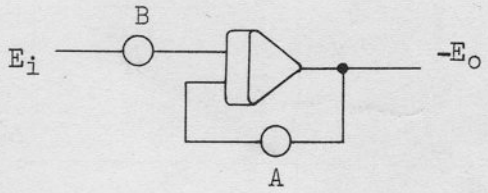
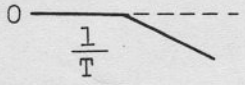
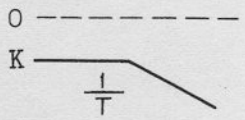
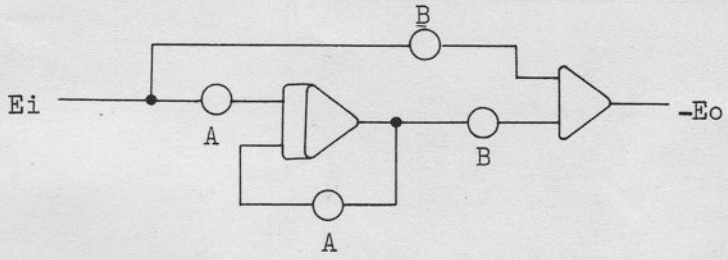
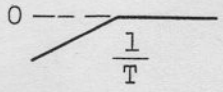
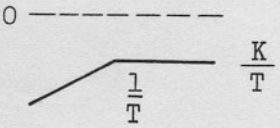
SIMPLIFIED DIAGRAM

$0 \leq X \leq +100$
or $-100 \leq X < 0$

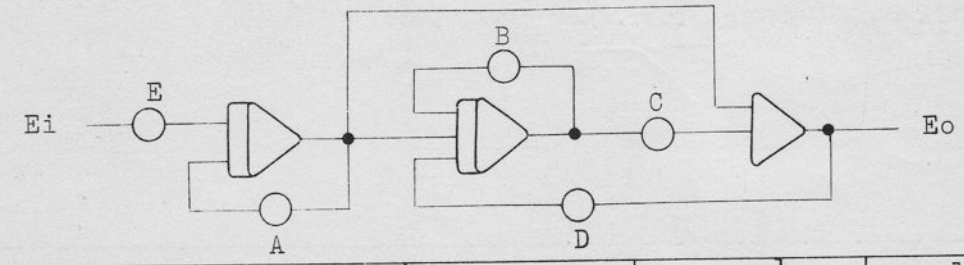
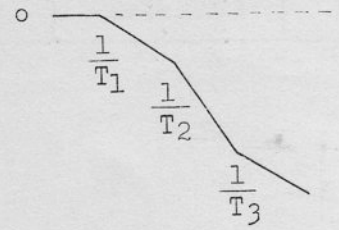
$-100 \leq F(X) \leq +100$

THE ABOVE DIAGRAMS SHOW POSITIVE INPUT CIRCUIT

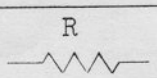
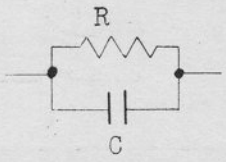
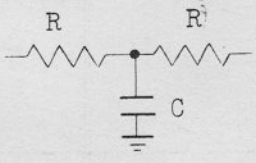
(a) The following Table contains examples of amplifier circuits for simulating transfer functions. A more complete listing may be found in Jackson, A.S.: "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960

NO.	BODE PLOT	TRANSFER FUNCTION	TIME CONSTANTS	GAINS
				
1		$\frac{1}{1+Tp}$	$T = \frac{1}{A}$	$A=B=\frac{1}{T}$
2		$\frac{X}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = AK$
				
3		$\frac{K_p}{1 + T_p}$	$T = \frac{1}{A}$	$A = \frac{1}{T}$ $B = 1$
4		$\frac{T_p}{1 + T_p}$	$T = \frac{1}{A}$ $K = BT$	$A = \frac{1}{T}$ $B = AK$

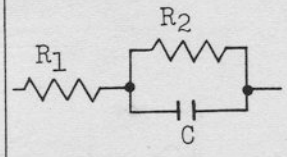
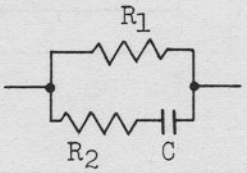
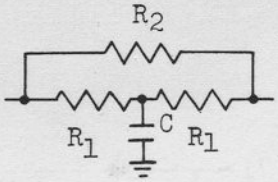
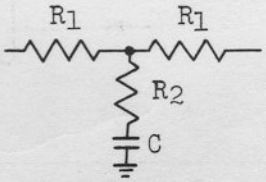
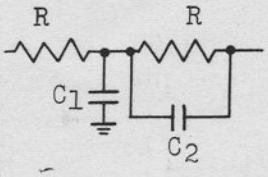
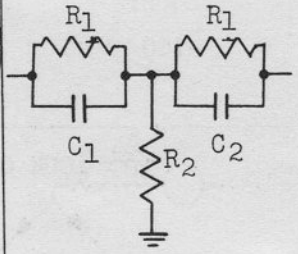
APPENDIX 7

NO.	BODE PLOT	TRANSFER FUNCTION	TIME CONSTANTS	GAINS
				
5		$\frac{1+T_3p}{(1+T_{1p})(1+T_{2p})}$	$T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$	$A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ $D = \frac{1}{C}(\frac{1}{T_3} - \frac{1}{T_2}) + 1$ $E = \frac{T_3}{T_1 T_2}$

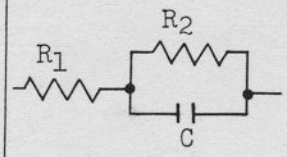
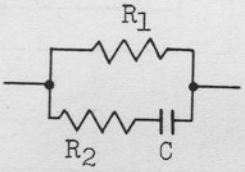
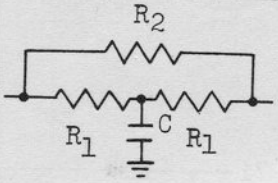
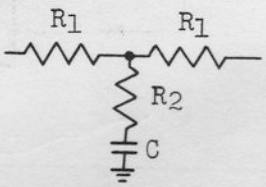
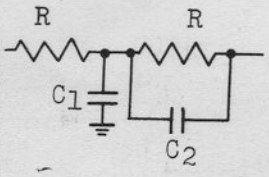
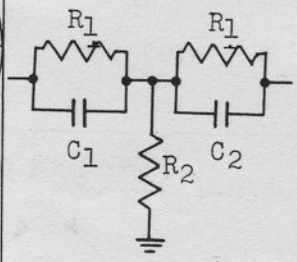
(b) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S.: "Analog Computation", and Fifer, S.: "Analog Computation".

NO.	Yss SHORT-CKT. ADMITTANCE	NETWORK	
1.	$\frac{1}{A}$		$A = R$
2.	$\frac{1 + pT}{A}$		$A = R$ $T = RC$
3.	$\frac{1}{A(1 + pT)}$		$A = 2R$ $R = \frac{RC}{2}$

APPENDIX 7

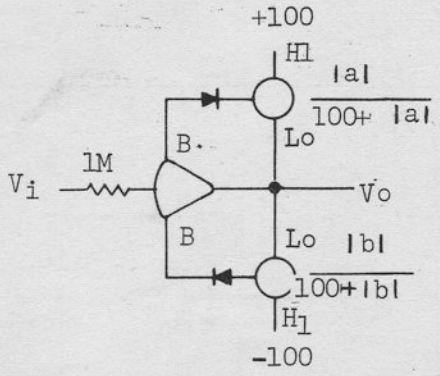
NO.	Yss SHORT-CKT. ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$ $\theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$ $\theta < 1$		$A = R_1$ $T = (R_1 + R_2)\, C$ $\theta = \frac{R2}{R_1 + R_2}$
6.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = \frac{2R_1R_2}{R_1 + R_2}$ $T = \frac{R_1 D}{2}$ $\theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R_1$ $T = (R + \frac{R_1}{2})\, C$ $\theta = \frac{2R2}{2R_2 + R_1}$
8.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left(\frac{(1+pT1)(1+pT3)}{(1+pT2)}\right)$ $T_2 \leq T_1 \leq T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$

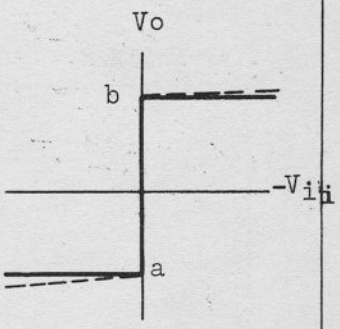
APPENDIX 7

NO.	Yss SHORT-CKT. ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$ $\theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$ $\theta < 1$		$A = R_1$ $T = (R_1 + R_2)\, C$ $\theta = \frac{R_2}{R_1 + R_2}$
6.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = \frac{2R_1R_2}{R_1 + R_2}$ $T = \frac{R_1 D}{2}$ $\theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R_1$ $T = (R + \frac{R_1}{2})\, C$ $\theta = \frac{2R_2}{2R_2 + R_1}$
8.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left(\frac{(1+pT1)(1+pT3)}{(1+pT2)}\right)$ $T_2 \leq T_1 \leq T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$

APPENDIX 8

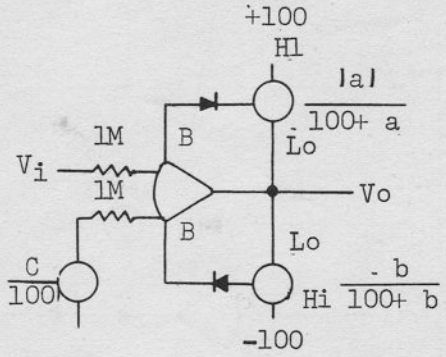
5.

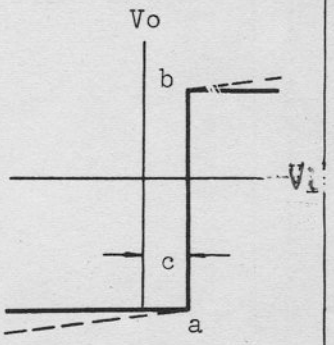




6.

BANG-BANG CIRCUITS





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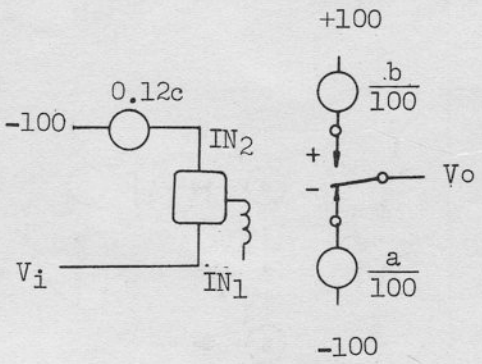
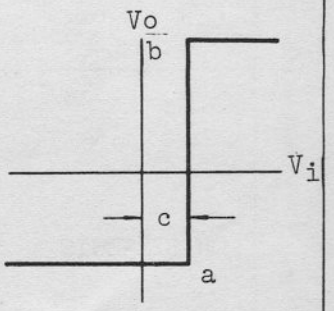
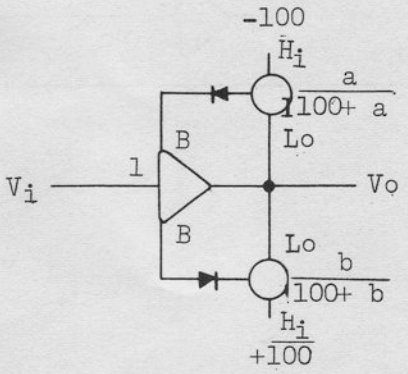
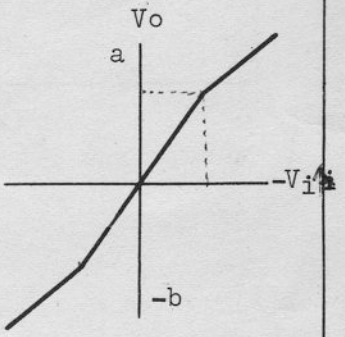




8.

SOFT LIMITER

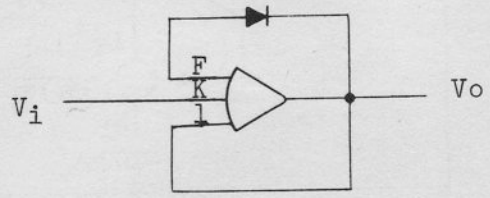


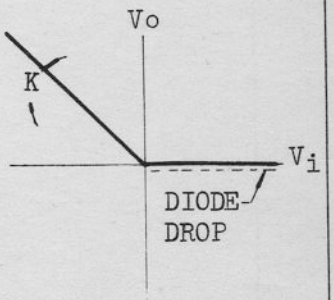


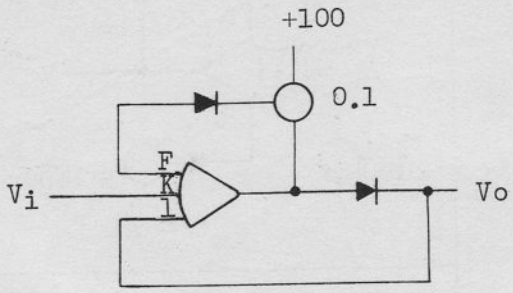
APPENDIX 8

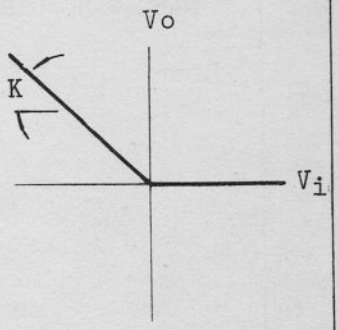
ZERO LIMIT HALF-WAVE RECTIFIER

10.









11.

HYSTERESIS